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Numerical Simulations and Designs for High-Efficiency Solar Cells

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Contents

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List of Publications

The following peer-reviewed journal articles have been published as a result of the work undertaken as part of this thesis.

[1] **Z. Yang**, W. Yang, X. Yang, J.C. Greer*, J. Sheng*, B. Yan, and J. Ye*. Device physics of back-contact perovskite solar cells. ***Energy Environmental Science***, 2020, 13:1753–1765.

[2] **Z. Yang**, Z. Liu, M. Cui, L. Lu, L. Chen, J. Sheng, W. Guo, X. Yang, Y. Zhao, W. Yang, J. C. Greer*, Y. Zeng*, B. Yan, and J. Ye*. Charge Carrier Dynamics for Silicon Oxide Tunneling Junction Mediating by Local Pinholes. ***Cell Reports Physical Science***, 2021, 2:100667.

[3] **Z. Yang**, J. Yan, W. Yang, Y. Zeng, J. Sun, X. Wang, X. Yang, J.C. Greer*, J. Sheng*, B. Yan, and J. Ye*. Back-contact structures for optoelectronic devices: Applications and perspectives. ***Nano Energy***, 2020, 78:105362.

[4] **Z. Yang**, H. Lin, K.W.A. Chee*, P. Gao*, and J. Ye*. The Role of Front-Surface Charges in Interdigitated Back Contact Silicon Heterojunction Solar Cells. ***Nano Energy***, 2019, 61:221–227.

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[1] X. Yang, Z. Ying, **Z. Yang**, J. Xu, W. Wang, J. Wang, Z. Wang, L. Yao, B. Yan, and J. Ye[*]. Light-Promoted Electrostatic Adsorption of High-Density Lewis Base Monolayers as Passivating Electron-Selective Contacts. *Advanced Science*, 2021, 8(5):2003245.

[2] F. Wu, H. Lin, **Z. Yang**, M. Liao, Z. Wang, Z. Li, P. Gao[*], J. Ye[*], and W. Shen[*]. Suppression of Surface and Auger Recombination by Formation and Control of Radial Junction in Silicon Microwire Solar Cells. *Nano Energy*, 2019, 58:817–824.

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List of Abbreviations

PV: photovoltaic

c-Si: crystalline silicon

BSF: back-surface field

PCE: power conversion efficiency

PERC: passivated emitter and rear cell

TOPCon: Tunnel Oxide Passivating Contact

a-Si:H: hydrogenated amorphous silicon

poly-Si: polycrystalline silicon

IBC: interdigitated back contact

QIBC: quasi-interdigitated back contact

SHJ: silicon heterojunction

SCs: solar cells

POLO: polysilicon on oxide

TMO: transition metal oxides

MoO_x: molybdenum oxide

VO_x: vanadium oxide

WO_x: tungsten oxide

PEDOT:PSS: poly(3,4-ethylene dioxythiophene):poly(styrenesulfonate)

HTL: hole-transport layer

ETL: electron-transport layers

S_{eff}: surface recombination velocity

ρ_c: specific contact resistance

PSC: perovskite solar cell

J_{sc}: short-circuit current density

PDMS: polydimethyl siloxane

GRIN: Gaussian-type gradient-index

ITO: indium tin oxide

$MAPbI_3$: methylammonium lead iodide

PL: photoluminescence

OMeTP: 4-methoxythiophenol

ClTP: 4-chlorothiophenol

MAI: methylammonium iodide

CSC: carrier-selective contacts

PECVD: plasma-enhanced chemical vapor deposition

MgO_x: magnesium oxide

TiO_x: titanium oxide

TaO_x: tantalum oxide

MgF_x: magnesium fluoride

LiF_x: lithium fluoride

Cs_2CO_3: cesium carbonate

V_{oc}: open-circuit voltage

FSF: front-surface field

D_{it}: interface defect density

IQE: internal quantum efficiency

HIT: heterojunction with an intrinsic thin-layer

DPTF: dielectric passivation thin film

Al_2O_3: aluminium oxide

ALD: atomic layer deposition

SiN_x: silicon nitride

SiO_2: silicon dioxide

Q_f: charge density

D_{pin}: pinhole density

ARC: antireflective coating

PR: photon recycling

J: current density

ρ: charge density

D: electric displacement

B: magnetic induction intensity

E: electric field

H: magnetic field

ε: permittivity

μ: magnetic conductivity

α: extinction coefficient

κ: imaginary part of the refractive index

$\Phi_{AM1.5}$: spectral flux under AM1.5G

P_s: power flow

λ: wavelength

J_{ph}: photocurrent density

q: unit charge

h: Plank constant

c: speed of light in vacuum

ε_r: dielectric constant

V: electrostatic potential

n: electron concentration

p: hole concentration

N_d: ionized donor concentration

N_a: ionized acceptor concentration

n_t^+: donor trap density

n_t^-: acceptor trap density

J_n: electron current density

J_p: hole current density

μ_n: electron mobility

μ_p: hole mobility

D_n: electron diffusion coefficient

D_p: hole diffusion coefficient,

k_B: Boltzmann's constant

T: temperature

R: total carrier recombination rate

R_{rad}: radiative or direct recombination rate

B_{rad}: radiative recombination coefficient

R_{Aug}: Auger recombination rate

A_n: electron Auger recombination coefficient

A_p: hole Auger recombination coefficient

R_{SRH}: Shockley-Read-Hall recombination rate

τ_n: electron lifetime

τ_p: hole lifetime

R_{sur}: surface recombination rate

S_n: surface recombination velocity of electron

S_p: surface recombination velocity of hole

n_i is the intrinsic carrier concentration

n_t: bulk electron concentration of the trap state

p_t: bulk hole concentration of the trap state

n_{ts}: surface electron concentration of the trap state

p_{ts}: surface hole concentration of the trap state

N_t: bulk defect density

v_{th}: thermal velocity

σ: capture cross-section

a^-: anion concentration

c^+: cation concentration

J_{a-}: anion current density

J_{c+}: cation current density

μ_{a-}: anion mobility

μ_{c+}: cation mobility

D_{a-}: anion diffusion coefficient

D_{c+}: cation diffusion coefficient

φ_{bb}: blackbody radiation flux

Δn: excess minority carrier charge concentration

N_d: doping concentration

W_{Si}: thickness of Si substrate

τ_{eff}: effective lifetime

τ_b: bulk recombination lifetime

τ_{rad}: radiative recombination lifetime

τ_{Aug}: Auger recombination lifetime

τ_{SRH}: SRH recombination lifetime

Δn_{av}: average excess carrier density

$J_{maj,pin}$: majority carrier current across pinhole

$J_{min,pin}$: minority carrier current across pinhole

$J_{maj,tun}$: majority carrier current across oxide

$J_{min,tun}$: minority carrier current across oxide

n_0: equilibrium minority carrier density

ρ: bare resistivity of c-Si region

f: area fraction of pinhole

TLM: transfer length method

CSM: Cox and Strack method

MIS: semiconductor insulator metal

A^*: effective Richardson constant

P_t: tunneling probability

t_{ox}: oxide thickness

m_t: tunnel mass

n: ideal factor

$\hbar$: reduced Planck's constant

$\Delta\varphi_s$: barrier difference between conduction band and Fermi-level

$\Delta\varphi_e$: tunneling barrier height

u: displacement field

ρ: material density

σ: stress

t: time

ε: normal strain

γ: shearing strain

E: Young's modulus

v: Poisson's ratio

μ: shear modulus

θ: volume strain

ε_{th}: thermal strain tensor

α: thermal expansion coefficient

N_c: conduction band density

N_v: valence band density

EQE: external quantum efficiency

J_{loss}: current-density loss

P_e: escape probability

P_a: parasitic absorption probability

P_r: reabsorption probability

FF: fill factor

E_f: Fermi level

ΔV: potential differences

QSSPC: Quasi-Steady-State-Photoconductance

ECV: electrochemical capacitance-voltage

FIB: focused ion beam

TEM: Transmission Electron Microscopy

c-AFM: conductive Atomic Force Microscopy

W_{pin}: pinhole size

iV_{oc}: implied open-circuit voltage

MPP: maximum power point

FTO: fluorine doped tin oxide

Abs: absorption efficiency

R: reflection efficiency

FEM: finite-element method

PML: perfectly matched layer

χ: Electron affinity

E_g: Bandgap energy

CBO: conduction band offset

VBO: valence band offset

ZnO: zinc oxide

PCBM: [6, 6]-phenyl-C61-butyric acid methyl ester

Nb_2O_5: niobium pentoxide

$SrTiO_3$: strontium titanium oxide

ICBA: indene-C_{60} bisadduct

ICTA: indene-C_{60} tri-adducts

spiro-MeOTAD: 2,2',7,7'-tetrakis-(N,N-di-4-methoxyphenylamino)-9,9'-spirobifluorene

CuI: Copper iodide

Cu_2O: cuprous oxide

CuO: cupric oxide

P3HT: poly (3-hexylthiophene)

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Abstract

With the further increase of human demand for energy, the development of renewable energy has become crucial. Photovoltaic (PV) technology, particularly solar cells (SCs), has emerged as a promising renewable energy source. However, to unlock the full potential of SCs, it is essential to address the challenges of reducing costs and improving device efficiency. This doctoral thesis focuses on crystalline silicon (c-Si) and perovskite solar cells (SCs), including dopant-free interdigitated back contact (IBC) SCs, Tunnel Oxide Passivating Contact (TOPCon) SCs, and perovskite SCs.

Firstly, the thesis explores the design principles and related mechanisms of dopant-free IBC SCs. Numerical simulations reveal that device efficiency can be improved by optimizing the device *pitch* and area fill ratio, or by reducing surface recombination at the electron transport layer and *n*-Si interface. The impact of passivation quality and contact resistance on efficiency is demonstrated, indicating the potential for achieving an efficiency exceeding 24%. Additionally, the thesis investigates Si surface passivation mechanisms induced by electric fields inherent to the dielectric films and examines the impact of device properties on IBC SCs through well-designed numerical simulations.

Secondly, the thesis combines elaborate simulations with experiments to uncover the physical mechanism of polycrystalline silicon (poly-Si)/silicon oxide (SiO_x)/c-Si contacts. Numerical simulations are employed to review the charge-carrier transport mechanism in poly-Si/SiO_x/c-Si contacts, suggesting that the tunneling and pinhole transport mechanisms are present and interact with each other. A fundamental physical model that considers passivation and contact behavior simultaneously is established to evaluate the potential efficiencies of devices. Proof-of-concept devices with complete cell structures demonstrate high efficiencies, averaging beyond 23.5% for the annealing temperature of 820°C, indicating the combined effect of passivation and contact properties on device performance.

Thirdly, an advanced optical design by texturing the front-side glass using a gradient-index Gaussian-type structure is proposed for PSCs. Numerical simulations show that this design exhibits a broadband light-harvesting response, resulting in a remarkable photocurrent density of 23.35 mA/cm². The optical absorption and loss distributions are analyzed, suggesting that Gaussian-type structures can effectively reduce reflection loss to 2.55 mA/cm². Furthermore, a comprehensive model is developed by coupling the traditional photoelectric model of free charge-carriers with the ion model and photon cycling (PR) model to simulate the carrier generation/transmission/recombination process of IBC PSCs. Simulation results indicate that: 1) IBC PSCs can achieve higher current density than ordinary sandwich PSCs due to reduced parasitic absorption loss; 2) optimized parameters can lead to cell efficiencies exceeding 25%; 3) mobile ions, with a concentration greater than 10^{16} cm^{-3}, play a crucial role in altering the energy band, free carrier distribution, and spatial electric field within the perovskite layer, thereby influencing cell efficiencies; 4) the introduction of PR effect can effectively enhance the open-circuit voltages and device efficiencies.

Chapter 1 Introduction

1.1 Development of PV Technology

The survival and development of human beings are inextricably linked to energy, as all economic activities rely on a stable energy supply. Additionally, energy plays a crucial role in the exploitation and utilization of other resources. Presently, approximately 85% of the world's energy requirements are met by finite fossil fuels, which already pose significant environmental and health risks. Consequently, the urgent need to address the escalating energy demands has propelled the development of renewable energy sources. Among the various alternatives, solar cells (SCs) have gained increasing attention due to their environmental friendliness, abundant resources, and cost-effectiveness, making them the most promising renewable energy option. Consequently, the research and development of photovoltaic (PV) technology have experienced remarkable progress and widespread exploration in recent years.

According to the latest report from the International Energy Agency Photovoltaic Power Systems Programme (IEA PVPS), the global PV market continues to be dominated by renewable energy, experiencing a significant increase in global installations, reaching 173.5 GW in 2021.[1] **Figure 1.1** illustrates the remarkable growth, resulting in a cumulative capacity of 945.4 GW by the end of 2021.[1] This surge in PV production capacity has necessitated higher efficiency requirements for solar cells (SCs). Consequently, improving the efficiency of SCs has become a pressing challenge for both the scientific research community and the industry. Fortunately, in recent years, several high-efficiency SC technologies have emerged, constantly setting new records in cell efficiency.

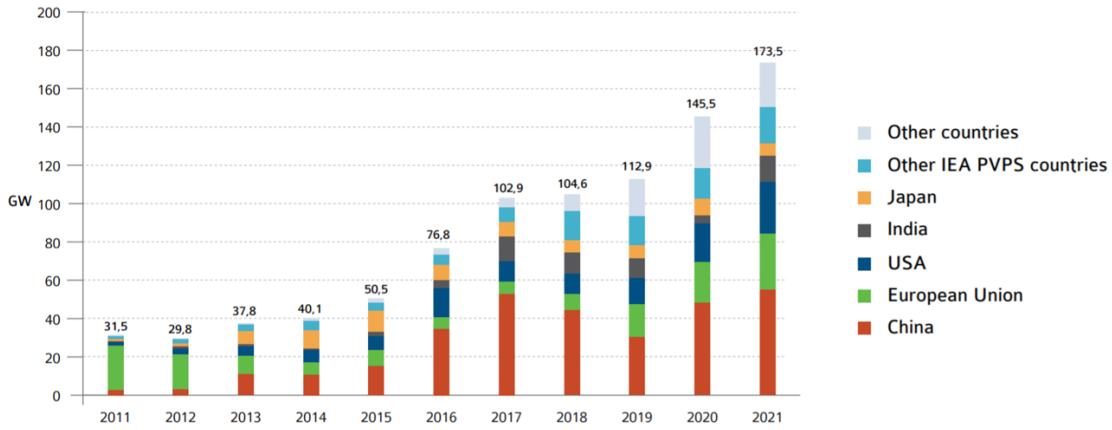

Figure 1.1 Evolution of annual PV installations.[1]

Generally, the development of photovoltaic (PV) technologies can be categorized into three generations based on materials and fabrication techniques. The first-generation PV technology relies on traditional silicon (Si) wafers, predominantly single-crystalline Si (c-Si) wafers and polycrystalline Si (mc-Si) wafers. The second-generation PV technology employs thin-film materials, such as copper indium gallium selenide (CIGS), amorphous silicon (a-Si), and cadmium telluride (CdTe). The third-generation PV devices encompass the latest advancements, including multi-junction solar cells (SCs), organic photovoltaics, dye-sensitized SCs, quantum dot SCs, and perovskite solar cells (PSCs), *etc*.[2]

Currently, mainstream silicon-based SC technology primarily consists of aluminum-back surface field (Al-BSF) technology and passivated emitter and backside cell technology (PERC). **Figure 1.2** illustrates the efficiency development history as depicted in a table released by the National Renewable Energy Laboratory (NREL).[3] In addition to the mainstream Si PV technologies, heterojunction (HJ) SCs exhibit significant advantages in terms of efficiency. By incorporating both HJ technology and interdigitated back contact (IBC) technology, the back-contact amorphous silicon HJ cell achieves a remarkable efficiency of 26.6%.[4] Recently, LONGi from China has increased the efficiency of HJ SCs to 26.81%.[5]

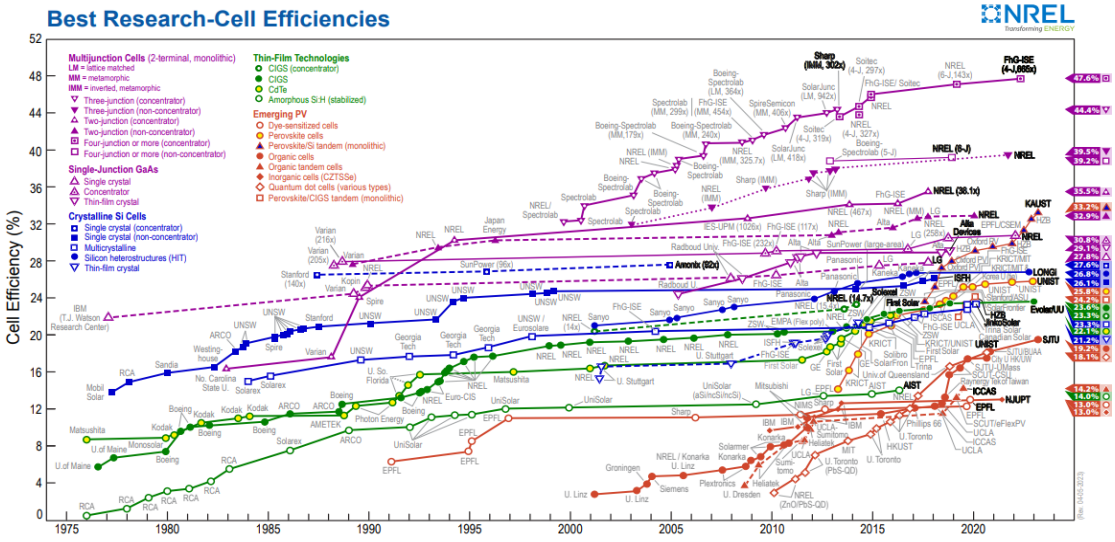

Figure 1.2 The chart of the best research-cell efficiencies by National Renewable Energy Laboratory (NREL).[3]

Recently, PSC technologies have emerged as a promising alternative for low-cost and high-efficiency PV technology. As PSC technology matures, its applications have become increasingly widespread, resulting in a rapid efficiency improvement from 3.8% in 2009 to 26.1% in 2023.[3] In 2009, Kojima *et al.* first proposed the application of the $CH_3NH_3PbI_3$ as the sensitizer in dye-sensitized SCs, receiving an efficiency of 3.8%.[6] Since then, extensive research and investigation have significantly improved the performance of PSCs. For instance, Park *et al.* enhanced the efficiency of PSCs to 6.5% in 2011 by replacing the acetonitrile solution with an ethyl acetate electrolyte and adjusting the perovskite layer thickness to 2-3 μm.[7] In 2012, Park *et al.* proposed the first all-solid-state PSCs, utilizing Spiro-OMeTAD as the transport material instead of the original liquid phase, achieving an efficiency of 9.7%.[8] This change improved device efficiency and stability. The same year, Snaith *et al.* suggested replacing iodine with chlorine in the $CH_3NH_3PbI_{3-x}Cl_x$ absorber layer, leading to better stability and carrier transport capabilities.[9] Additionally, they employed a simple and cost-effective solution technique to prepare a conductive aluminum trioxide (Al_2O_3) electron transport layer (ETL) instead of titanium oxide (TiO_2), resulting in improved efficiencies of 10.9%. Griitzel *et al.* introduced the two-step solution deposition method in fabricating perovskite films, yielding an efficiency of 15%.[10] Soon after, Snaith *et al.* utilized a

hybrid evaporation process to produce perovskite thin films, achieving a planar heterojunction PSC with an efficiency of 15.4%.[11] Yang *et al.* further improved the PSC efficiency to 19.3% by modifying the structure of the TiO_2 layer.[12] In 2016, Gratzel *et al.* incorporated poly(methyl methacrylate) (PMMA) into the perovskite layer to regulate the crystallization of the perovskite film, resulting in a certified efficiency of 21.02%.[13] In 2017, Seok *et al.* reduced deep defects by introducing excess iodide ions into $FAPbI_3$-based perovskite, achieving a certified efficiency of 22.1% for a small area.[14] Through persistent efforts from researchers, the efficiency of the latest certified PSC has reached 26.1% in 2023 as depicted in **Figure 1.2**.

1.2 c-Si Solar Cells

Currently, c-Si technologies account for over 95% of overall cell production.[1] However, conventional Al-BSF solar cells (SCs) have dominated the Si-based photovoltaic (PV) community in recent decades, but their market share has decreased due to limitations in power conversion efficiency (*PCE*). Industrial production of Al-BSF SCs achieves *PCEs* of 17%–19%, with a practical upper limit of approximately 20%. On the other hand, passivated emitter and rear contact (PERC) SCs, with industrial production efficiencies of 23–24%, have emerged as one of the most dominant PV technologies. The sustainability of Si-based PV technologies relies on continuous advancements in device efficiency, cost reduction, and the promotion of technological revolutions in device design.

For the c-Si PV technologies, there are inherent drawbacks, with the most prominent one being the direct contact of Si substrates with the subsequent metal electrodes. To address this issue, passivating contact designs, initially proposed in organic SCs, have been successfully adopted in Si-based devices.[15] These designs require high-level passivation to reduce minority-carrier recombination, while maintaining relatively low contact resistivity to facilitate majority-carrier transport.[16,17] Two representative technologies are a-Si/crystalline Silicon (c-Si) Heterojunctions (SHJ) and Tunnel Oxide Passivating Contact (TOPCon). In particular, IBC-SHJ SCs, which combine the high-level passivation provided by a-Si film with an interdigitated back contact (IBC) architecture, have achieved a high efficiency of 26.7%.[4] However, this type of Si-based PV technology is limited by a complex fabrication process flow and capital-intensive equipment, despite its tempting potential efficiency. Therefore, TOPCon technology has attracted a lot of attention as it has the potential to achieve high efficiency with a simpler fabrication process.

Additionally, another important passivation and contact technology, featuring a dopant-free approach, has also garnered significant interest due to its relatively simple

preparation process and high potential in device efficiency.

1.2.1 Dopant-Free IBC c-Si Solar Cells

Over the last three decades, there has been significant progress in Si-based PV technology. For efficient c-Si PV, it is necessary to have appropriate functional materials, as well as advanced structural design. Among these designs, the interdigitated back contact (IBC) configuration is the best choice for high-efficiency c-Si SCs. With the integration of two electrodes with different polarities on the rear side of the device, the optical loss caused by shadowing on the front surface can be eliminated, leading to a higher potential in terms of short-circuit current density (J_{sc}) and *PCE*. Despite the potential of IBC technology in enhancing device efficiency, there are some challenges. The complexity of the process needed to achieve this efficiency comes at a cost, which lowers the efficiency/cost ratio, and as a result, holds back the commercialization progress of IBC c-Si PV devices.

The efficiency evolution of typical Si-based IBC SCs is depicted in **Figure 1.3**, while the corresponding device configurations are presented in **Figure 1.4**. **Figure 1.3** clearly demonstrates that the power conversion efficiencies (*PCEs*) of polysilicon on oxide (POLO) and IBC-SHJ SCs are higher compared to other cases. Notably, the IBC-SHJ SCs achieved the high efficiency of 26.7% in 2017.[4] Since then, the efficiency of POLO-IBC SCs has shown a rapid increase, surpassing 26%.[18] Although the efficiency of dopant-free IBC SCs is experiencing significant growth, its current efficiency remains low, making it challenging to compete with the aforementioned technologies in the present stage. However, with the backing of new technologies, there is a promising potential to achieve breakthrough efficiency and improved competitiveness within the c-Si PV community.

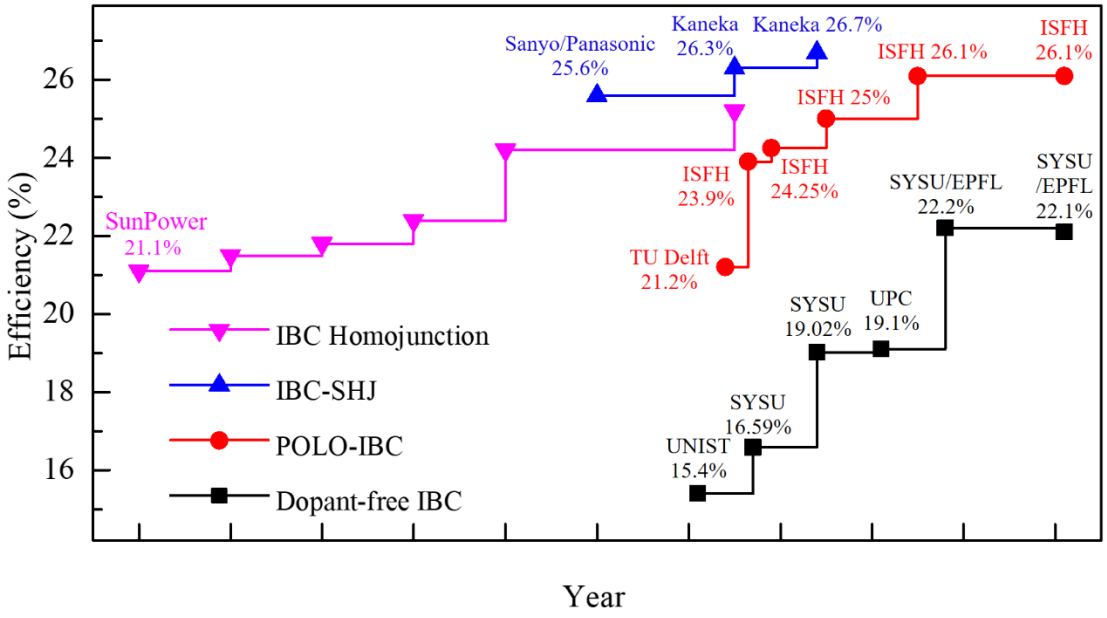

Figure 1.3 Efficiency evolution of Si-based SCs with IBC design.[19]

The concept of carrier-selective contacts, incorporating a dopant-free design, initially gained widespread use in organic devices before being successfully introduced into c-Si SCs.[20-23]. This approach has yielded remarkable outcomes thus far. By developing dopant-free Si SCs, the high-temperature doping process can be eliminated, offering several advantages over traditional Si-based SCs. In the case of dopant-free Si SCs, a variety of hole-transport layers (HTLs) with high work-function, such as tungsten oxide (WO_x),[24] molybdenum oxide (MoO_x),[24,25] vanadium oxide (VO_x),[24] cuprous oxide (Cu_2O),[26] as well as poly(3,4-ethylene dioxythiophene):poly(styrenesulfonate) (PEDOT:PSS),[27-30] have been extensively employed. Additionally, low work-function electron-transport layers (ETLs) composed of alkali/alkaline earth metal salts, metals/metal oxides, and other materials have found wide application.[30-33] These combinations of HTLs and ETLs offer promising avenues for fabricating fully dopant-free IBC Si-based SCs. Through the utilization of these materials, simple fabrication methods can be employed, leading to the realization of highly efficient c-Si SCs. By combining the IBC design with the use of the aforementioned materials, fully dopant-free IBC Si-based SCs can be manufactured, offering a promising pathway towards achieving high efficiency.

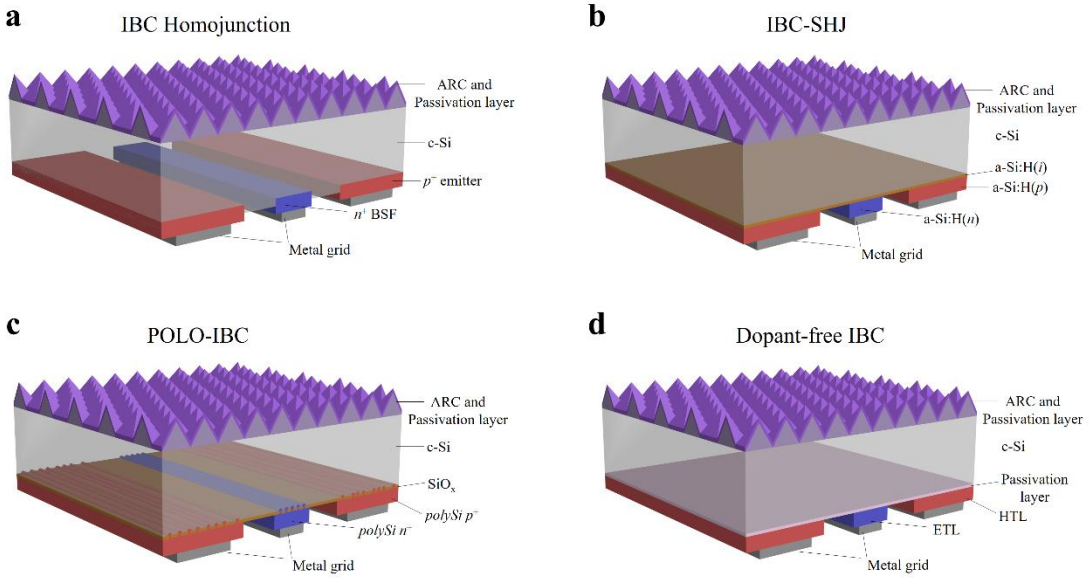

Figure 1.4 Sketch maps of c-Si SCs with different-types of designs: (a) IBC homojunction, (b) IBC-SHJ, (c) POLO-IBC, and (d) dopant-free IBC SCs.[19] For IBC and dopant-free IBC SCs, the inclusion of an ultra-thin passivation layer, such as a-Si:H(*i*), may be necessary to guarantee high-quality passivation.

In the context of IBC structures, the parasitic absorption of functional materials, specifically the HTL and ETL layers, on the front side of devices can be effectively mitigated. This characteristic allows for a wider range of functional materials to be used in the fabrication of dopant-free IBC c-Si solar cells (SCs). Consequently, these cells exhibit a high tolerance towards the selection of functional materials. The photoelectrical properties of IBC Si-based SCs with a dopant-free design are primarily influenced by two crucial factors: passivation quality and contact resistance. These factors are determined by the choice of ETL and HTL layers, as well as the additional interface passivation layer. Notably, the carrier transport route is a key distinction compared to conventional devices. In IBC-based SCs, carriers must be transported both horizontally and longitudinally to reach the respective electrodes. Therefore, the region separating the ETL and HTL layers, known as the gap region, plays a vital role in the performance of the device, including its passivation quality and structural characteristics.

The breakthrough achievement of fully dopant-free carrier-selective contacts, also known as dopant-free asymmetric heterocontacts (DASH), was reported by Bullock *et al.* in 2016. They demonstrated a high efficiency of 19.4% for dopant-free IBC c-Si solar cells, marking the first report of efficiency exceeding 19%.[16] Building upon the identical structural design, they further increased the efficiency of this type of Si-based devices to 20.7% while maintaining high thermal stability.[34] In a normal sandwich structure, Zhong *et al.* reported a remarkable efficiency of 21.4%.[35] More recently, through optimization of the *pitch* size and passivation quality, dopant-free IBC c-Si SCs have achieved efficiencies exceeding 22%.[36] This suggests a flexible approach for developing high-efficiency Si-based devices using relatively simple processes at a low cost. These advancements demonstrate the potential of dopant-free IBC c-Si solar cells to achieve higher efficiencies, paving the way for the development of cost-effective and efficient Si-based devices.

Considerable research efforts have been dedicated to improving the performance of dopant-free IBC SCs through the use of advanced materials and novel preparation methods. For instance, in 2016, Kwanyong *et al.* utilized MoO_x as the HTL and LiF_x as the ETL for the dopant-free IBC SCs. By incorporating a nanohole design for front light trapping, they achieved moderate efficiency (15.4%), moderate V_{oc} (561 mV), moderate J_{sc} (36.8%), and moderate *FF* (74.6%).[37] Shen's group conducted a study on three commonly used hole transport layers (VO_x, WO_x, and MoO_x) for dopant-free IBC SCs. They concluded that devices employing VO_x as the HTL achieved the highest efficiency of 16.59%, surpassing MoO_x (15.09%) and WO_x (12.44%).[38] The superior device performance of VO_x-based IBC SCs was primarily attributed to the favorable electrical characteristics of the VO_x/*n*-Si contact, which exhibited low surface recombination ratio (S_{eff}) of 138 cm/s and low contact resistivity (ρ_c) of 34 $m\Omega \cdot cm^2$ at the VO_x/*n*-Si interface.

A recently reported dopant-free IBC SC by Masmitja *et al.* employed Ni and VO_x as hole selective contacts, resulting in low J_0 (175 fA/cm^2), low ρ_c (115 $m\Omega \cdot cm^2$), and

remarkable efficiency of 19.7% even without additional passivation materials.[39] Additionally, they introduced a novel ultrathin aluminum oxide (Al_2O_3)/TiO_2/Mg ETL fabricated through atomic layer deposition (ALD) and thermal evaporation, which exhibited high device performance with ultra-low ρ_c (2.5 m$\Omega\cdot cm^2$), low S_{eff} (40 cm/s), and high efficiency (19.1%).[40] Furthermore, Shen *et al.* proposed a TMO/metal/TMO HTL to enhance the contact performance at the HTL/*n*-Si interface. They achieved low ρ_c (0.04 m$\Omega\cdot cm^2$) and remarkable efficiency (19.02%) for dopant-free IBC SCs by integrating a 2 nm-thick LiF_x ETL and an 8 nm-thick thermal-evaporated VO_x/Au/VO_x HTL.[41] Similarly, they demonstrated a stable efficiency of 15.8% using a 5 nm-thick CrO_x film as a replacement for the 8 nm-thick VO_x film.[42]

Despite numerous achievements, the attainment of high device performance remains a challenge due to poor interface passivation between c-Si/ETL and c-Si/HTL contacts. To address this issue, high-quality passivation layers such as a-Si:H(*i*) have been extensively employed. For instance, Li *et al.* demonstrated a 20.24% efficient SC with dopant-free and IBC designs by incorporating MoO_x HTL, SiO_x/TiO_2 ETL, and high-level a-Si:H(*i*) films for interface passivation.[43] Furthermore, Ye *et al.* reported a 20.1% efficiency for Si-based dopant-free IBC SCs utilizing MoO_x HTL, LiF_x ETL, and a-Si:H(*i*) layers in conjunction with improved two-step hard masks alignments.[44] Additionally, Wu *et al.* achieved high-performance IBC SCs with dopant-free designs, obtaining efficiencies of 22.2%[36] and 22.1%[45] by employing a 1.5 nm MgF_x film and a 1.5 nm-thick MgF_x/a 20 nm-thick Mg ETL contacts, respectively.

To simplify the fabrication process of high-efficiency dopant-free IBC SCs, more advanced strategies for constructing IBC structures should be explored. For instance, Lin *et al.* proposed a novel quasi-interdigitated back contact (QIBC) structure, which demonstrated a proof-of-concept dopant-free IBC SC with a 16.3% efficiency.[46] In this structure, the HTL and ETL consisted of a thin PEDOT:PSS layer and a 1 nm-thick MgO_x film, respectively. A MgO_x/Al stack was covered by an insulating polymer and a PEDOT:PSS layer across the entire region. By addressing edge leakage and reducing

carrier recombination in the gap region, the dopant-free QIBC SCs achieved efficiencies surpassing 20%.[47]

1.2.2 TOPCon Solar Cells

Since it was first reported by Fraunhofer in 2013,[48] TOPCon device has attracted much attention in the PV community.[49-52] **Figure 1.5** illustrates the schematic diagram of TOPCon SCs.

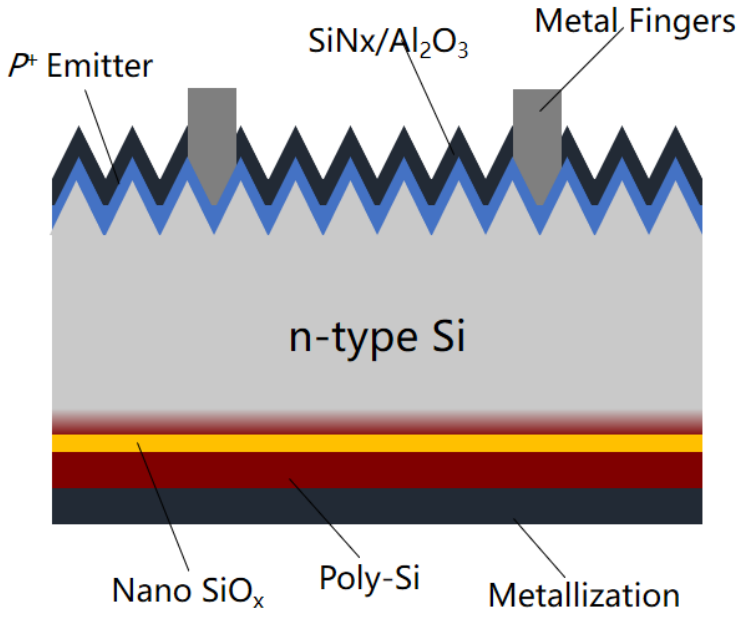

Figure 1.5 Sketch map of TOPCon SCs.

Due to its compatibility with conventional passivated emitter rear contact (PERC) production lines, the TOPCon technology has garnered significant interest in both academic and industrial fields. In just five years, Fraunhofer achieved remarkable efficiency improvements, with TOPCon devices reaching 25.7% efficiency in 2018.[53] Recently, they reported device efficiencies exceeding 26%.[54] The popularity of TOPCon technology extends beyond Fraunhofer, with researchers from various foreign and domestic institutions also favoring its utilization, leading to extensive studies. For instance, Tao *et al.* from Georgia Tech. achieved an impressive efficiency of 21.2% on

a large area of 239 cm^2 using back-contacted TOPCon technology in 2016.[55] Peibst *et al.* from ISFH, utilizing *n*-type TOPCon or POLO junctions, achieved excellent passivation quality with a low J_0 of 0.6 fA/cm^2 and a high iV_{oc} of 748 mV in 2016.[56] Kim *et al.* from Korea University successfully obtained a high iV_{oc} surpassing 740 mV on an *n*-type Si wafer by optimizing the annealing conditions to control oxide stoichiometry in 2017.[57] CNITECH achieved a high-quality TOPCon junction in 2018, achieving a high iV_{oc} of 731 mV, a low J_0 of 6 fA/cm^2, and a cell efficiency of 21.12%.[58]

Currently, TOPCon solar cells are primarily fabricated on *n*-type silicon wafers. However, the cost of *n*-type silicon is considerably higher compared to *p*-type silicon. Consequently, efforts are being made to develop TOPCon cells using *p*-type silicon wafers as substrates. Nevertheless, passivating p-type silicon wafers poses greater challenges compared to *n*-type silicon. Notably, Fraunhofer achieved high efficiencies of up to 24.3% and 26% for *n*-type TOPCon devices featuring *p*-type Si wafers and rear-junction designs in 2017 and 2020, respectively.[59,60]

1.3 Perovskite Solar Cells

In the past decade, perovskite solar cells (PSCs) have emerged as a prominent area of research due to the distinctive photoelectrical benefits offered by perovskite thin films.

Thus far, significant progress has been made, with single junction PSCs achieving an impressive efficiency exceeding 26%. However, further enhancement of efficiency using traditional methods has become increasingly challenging. Therefore, one of the most effective approaches is to employ advanced structural designs, including optical design and interdigitated back contact (IBC) structures. These strategies have proven to be highly effective in improving the performance of PSCs.

1.3.1 Optical Designs

While solar cells (SCs) have made significant advancements in efficiency over the past decade, the issue of optical loss caused by front reflection, resulting from the use of flat structural designs, remains a challenge that requires advanced optical design to enhance optical response and device performance. In the case of perovskite solar cells (PSCs), reducing optical losses has been recognized as a highly effective approach to increase short-circuit current densities (J_{sc}s) and efficiencies.

Numerous methods of optical management have been explored for PSCs.[61-65] For instance, Song *et al* implemented a diffraction grating on the bottom side of the perovskite film to enhance infrared optical response. This led to improvements in device J_{sc} and efficiency from 21.67 to 23.11mA/cm^2 and from 16.71% to 19.71%, respectively.[61] Li *et al.* proposed a double-layer optical design consisting of a TiO_2 grating covered by a polydimethyl siloxane (PDMS) anti-reflection layer (ARC), which effectively improved the optical properties of the device, resulting in a 1.2 mA/cm^2 increase in J_{sc}.[62] Zhang *et al.* utilized crater-like structures across all layers of the PSCs, achieving an 18.6% efficiency for a thin PSC with a $MAPbI_3$ absorption layer of only 200 nm.[63]

Although these advanced designs have shown promise in enhancing device properties, they also present certain drawbacks, such as increased process complexity. Additional steps involved in texturing functional layers and perovskite layers can raise process

difficulties and potentially degrade the film quality, leading to poorer device performance. Furthermore, the highest reported efficiency for PSCs with additional optical structures is 23%, which falls short of the highest value reported for flat PSCs.[66-69] In traditional flat-configured PSCs, optical losses primarily stem from reflection loss at the front surface of the devices.[70] Therefore, mitigating front-surface reflection loss is crucial for effectively boosting optical absorption in the perovskite layer and consequently improving device efficiency. However, achieving optical gains without resorting to textured designs for functional materials and the perovskite layer is a challenging task. In addition to PSCs, advanced structures for optical management have been widely employed in c-Si-based solar cells.[71-74] For example, Lin *et al.* achieved a Gaussian-type gradient-index (GRIN) profile on the c-Si substrate using a teepee-like photonic crystal structure, resulting in a notable optical response with an average reflection of approximately 0.7% in the wavelength range of 400 to 1000 nm.[74]

1.3.2 IBC Perovskite Solar Cells

While PSCs with interdigitated back contact (IBC) structures exhibit promising efficiency potential, as depicted in **Figure 1.6**, the fabrication process becomes more complex, particularly for PSCs with thin perovskite absorption layers. Achieving high-efficiency IBC PSCs necessitates a significant carrier diffusion length to accommodate the large pitch size inherent in IBC designs. However, perovskite films typically do not possess such long carrier diffusion lengths, making it necessary to reduce the pitch size, including the hole transport layer (HTL), electron transport layer (ETL), and the gap size, to only a few microns. This reduction poses a considerable challenge. Moreover, the resulting intricate process might compromise the passivation of perovskite films, further adding to the difficulties. In addition to the challenges in pitch size reduction, the electrical properties of the ETL/perovskite and HTL/perovskite interfaces play a critical role in determining the performance of IBC PSCs. Optimizing these interfaces becomes more demanding, further contributing to the complexity of achieving high-

efficiency IBC PSCs.

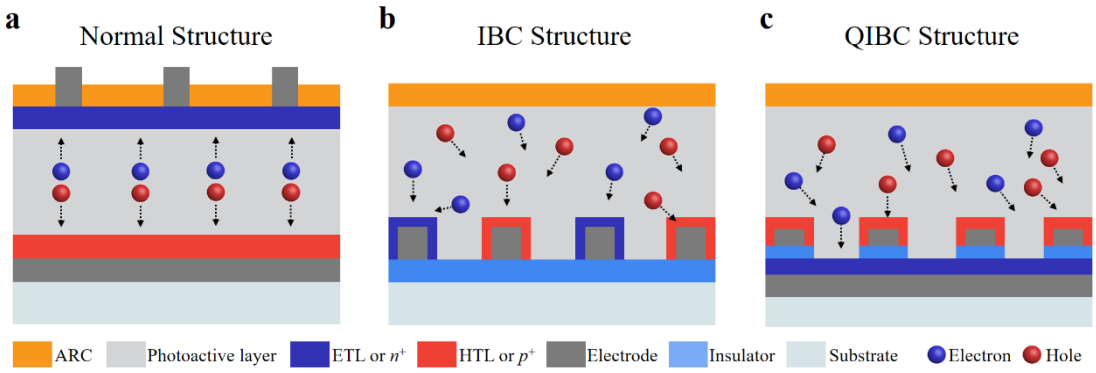

Figure 1.6 Schematic diagrams of PSCs with the different structures.[19]

In traditional IBC c-Si SCs, a high-temperature annealing process is typically required, but this approach is not applicable for IBC PSCs. In the case of PSCs, the inherent poor carrier diffusion length of perovskite films necessitates advanced structural designs to enhance carrier transport, suppress carrier recombination, and improve carrier collection. Therefore, designing feasible electrode structures is crucial for fabricating high-efficiency IBC PSCs. Many studies have been conducted in response to this challenge.[75] For instance, a newly developed honeycomb-shaped electrode structure was proposed for carrier collection in IBC PSCs.[76-78] By optimizing the electrode sizes, these IBC PSCs exhibited high tolerance to interface defects, resulting in excellent J_{sc} values of 16.4 mA/cm^2 and stable device efficiencies of 4%.[79] Building upon similar structures, device performance can be further improved by incorporating a dipole-field-assisted design.[78] Furthermore, a semi-transparent quantum IBC PSC with an indium tin oxide (ITO) substrate was demonstrated using the same configuration.[80] Additionally, Lidzey *et al.* employed micron-sized grooves to construct quantum IBC PSCs. In this approach, the methylammonium lead iodide ($MAPbI_3$) perovskite absorption layer was deposited within the grooves and then covered by both *n*-type and *p*-type selective materials.[81] Consequently, they achieved an efficiency of 7.3% for the IBC PSC with a single groove, and over 4% efficiency with a high open-circuit voltage

(V_{oc}) of 15 V for the multiple groove micro-modules. This innovative method offers a promising approach to fabricating flexible perovskite-based devices.

To further enhance the properties of IBC-based PSCs, it is crucial to improve the efficiency of charge extraction. Typically, carrier transport can be evaluated through photoluminescence (PL) and photocurrent mapping measurements.[82] By introducing self-assembled monolayers, such as 4-methoxythiophenol (OMeTP) and 4-chlorothiophenol (ClTP), on two different polarities, the efficiency of charge extraction can be effectively enhanced.[83] By combining high-quality single crystal perovskite films with the dipole fields at the Au/perovskite interface, a photovoltage of 600 mV and a photocurrent of 12.1 mA/cm^2 were achieved. Investigations on the photoelectrical properties, including photocurrent densities, V_{oc}, lifetimes, and trap densities, revealed that increasing perovskite cluster sizes can promote carrier transport and extraction. Improving perovskite quality or reducing pitch size can also enhance device performance.[84] By introducing a thin layer of methylammonium iodide (MAI) for high-quality passivation, a stable IBC PSC with an 80 meV enhancement in surface potential and an efficiency of 11.52% were achieved with a pitch size of 50 μm.[85] These IBC PSCs also demonstrated excellent long-term operational stability, even under 200 hours of light exposure. Leveraging the long carrier diffusion lengths of single crystal organometallic trihalide perovskite, Huang *et al.* reported a lateral design with metal/organometal trihalide perovskite/metal configuration, where single crystal perovskite exhibited a strong piezoelectric effect.[86] After that, they further demonstrated a thin multicrystal $MAPbI_3$ by using a low-temperature solution process, achieving a 5.9% efficiency for IBC PSCs.[87] Recently, Tainter *et al.* achieved prolonged charge transport in a metal-halide perovskite (polycrystalline) layer, with a carrier lifetime exceeding 12 μm and a measured recombination rate of 2 cm/s through photocurrent and PL measurements.[88] This resulted in a high J_{sc} value of 18.4 mA/cm^2 for IBC PSCs.

Despite significant progress, the device performance of IBC PSCs still remains poor.

To gain a deeper understanding of the physical and mechanistic aspects of IBC PSCs, theoretical investigations are necessary. Fang *et al.*, through simulations, found that IBC PSCs exhibit higher efficiency potential compared to their counterparts with traditional sandwich designs, assuming identical parameters such as diffusion length and *pitch* size.[89] Further optimization of electrical parameters led to a predicted efficiency of 28.27% for IBC PSCs. Simulations by Ma and Shalenov *et al.* also confirmed the superior efficiency of IBC PSCs compared to normal sandwich PSCs, provided a small contact width and high-quality perovskite film are ensured.[90,91] In the case of quasi-interdigitated back contact (QIBC) PSCs, simulations predicted high optical gain. By texturing the perovskite layer on the front side, covered by a PMMA ARC layer with an optimized thickness of 75 nm, a high optical response with a photocurrent density of 24.03 mA/cm^2 can be expected.[92]

Moreover, IBC structures serve as a versatile tool for studying the device physics of perovskite-based devices. For instance, perovskite films on wafer-scale areas were fabricated using a simple one-step roll-imprinting method, resulting in outstanding carrier mobility (45.64 cm^2/Vs). This approach yielded IBC PSCs with an efficiency of 4.83%, providing a facile way to prepare large-area IBC PSCs.[93]

1.4 Objective and Thesis Outline

The main objective of this thesis is to use advanced simulation technologies and well-designed experiments to investigate the charge-carrier transport mechanism, design advanced optical structures, optimize photoelectrical parameters, and predict the performance of crystalline silicon (c-Si) and perovskite solar cells (SCs). The thesis is

organized into the following chapters.

Chapter 1 provides an introduction to the background and development of photovoltaic devices, including dopant-free c-Si SCs, TOPCon SCs, and perovskite SCs. The research status, problems, and challenges associated with these photovoltaic devices are emphasized. Furthermore, the research objectives and significance of these types of PV devices are highlighted.

Chapter 2 presents a summary of the foundational models and equations used for simulating the photoelectric performance of PV devices by integrating optical and electrical models. The processes of ion migration and photon recycling (PR) effects within perovskite devices are explained. Subsequently, passivation and contact models are developed to extract passivation-quality and contact resistance properties.

Chapter 3 focuses on the design principles of dopant-free Si-based IBC solar cells through well-designed numerical simulations and experiments. The structural parameters, such as pitch size and size ratio, and electrical parameters, including surface passivation quality, doping concentration, and contact properties, are extensively investigated. Furthermore, the thesis aims to elucidate the Si surface passivation mechanism in an IBC c-Si SC, which occurs as a result of the electric field induced by charges present in the dielectric films. This investigation involves examining the distributions of energy, potential, internal electrical field, charge-carrier concentration, and carrier density to provide a comprehensive understanding of the passivation process.

Chapter 4 provides a clarification of the potential physical mechanism underlying the poly-Si/SiO_x/c-Si contact through a combination of elaborate simulations and experiments. It confirms the occurrence of local SiO_x fracture with pinholes and determines the density of these pinholes. The process of pinhole formation is elucidated by investigating the stress resulting from thermal expansion. By analyzing the pinhole density/size and SiO_x thickness, the carrier transport mechanism for the poly-Si/SiO_x/c-

Si contact, dominated by tunneling or pinholes, is revealed. A fundamental physical model is established to evaluate the potential efficiencies of devices by considering both passivation and contact behavior simultaneously. Additionally, a detailed current-recombination analysis and prediction of a specific roadmap for improving device efficiency are carried out.

Chapter 5 focuses on investigating the photoelectrical properties of an IBC-based perovskite solar cell through comprehensive simulations. The carrier generation, transport, and recombination processes in such an IBC perovskite solar cell are clarified, and electrical parameters such as passivation quality, mobility, and doping concentration are thoroughly investigated. The carrier transport mechanism in this type of IBC perovskite solar cell is elucidated, and the impact of ion migration and photon recycling (PR) effects on device performance is assessed. Moreover, to reduce reflection losses in flat perovskite solar cells, a Gaussian-type optical structure involving the texturing of front glass is proposed, and the structural parameters, light-trapping mechanism, and angle response are thoroughly examined.

Finally, in Chapter 6, the key contributions of this thesis concerning c-Si SCs and perovskite SCs are summarized. Furthermore, an outlook is provided to highlight the anticipated future development of c-Si SCs and perovskite devices.

Chapter 2 Theoretical Background

This chapter provides an introduction to the foundational models used in the thesis, which include the carrier-transport model, and passivation contact property extraction model. The carrier-transport model addresses the processes of carrier generation, transport, recombination, and collection. The passivation contact model is developed to extract properties related to passivation quality and contact resistance.

2.1 Carrier-Transport Model

In this section, detailed explanations are provided for the charge carrier transport models, which encompass the optical model, electrical model, ion migration model, and photon recycling model.

2.1.1 Optical Model

In the 1860s, Maxwell formulated a comprehensive theory of electromagnetic fields based on the work of his predecessors.[94] He predicted the existence of electromagnetic waves and derived the formula for wave velocity. Maxwell's equations, which describe the behavior of electromagnetic fields, are as follows:

$$\begin{cases} \nabla\times\boldsymbol{H} = \frac{\partial \boldsymbol{D}}{\partial t} + \boldsymbol{J} \\ \nabla\times\boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \\ \nabla\cdot\boldsymbol{B} = 0 \\ \nabla\cdot\boldsymbol{D} = \rho \end{cases} \tag{2.1}$$

where $\boldsymbol{J}$ and ρ are the body current-density vector and density, respectively, $\boldsymbol{H}/\boldsymbol{E}/\boldsymbol{B}/\boldsymbol{D}$ is the vector of magnetic-field/electric-field/magnetic-induction-intensity/electric displacement. In an isotropic medium, the equation of matter can be expressed as:

$$\boldsymbol{D} = \varepsilon\boldsymbol{E}; \quad \boldsymbol{B} = \mu\boldsymbol{H} \tag{2.2}$$

where ε/μ is permittivity/magnetic-conductivity. In the optical simulation, the aforementioned equations were solved to determine the spatial distribution of electric and magnetic fields. This enables the calculation of optical response, including reflection, absorption, and loss. Moreover, the optical information obtained allows for the determination of carrier generation distribution. In one-dimensional (1D) carrier-transport simulations, carrier generation is often assumed to follow a uniform distribution based on the Lambert-Beer model.[95] However, this approach may not be sufficiently accurate in many cases, especially for 2D nanostructures. In such cases, where incident light undergoes multiple reflections and resonances, a detailed electromagnetic-based optical simulation is necessary. The frequency-dependent spatial carrier generation rate, denoted as 'g', can be expressed as follows:[96]

$$g\,(x, y, z, \lambda) = \alpha(\lambda)\Phi_{AM1.5}(\lambda)\; P_{\mathrm{s}}(x, y, z, \lambda) \tag{2.3}$$

$$P_{\mathrm{s}}\,(x, y, z, \lambda) = \sqrt{|P_{\mathrm{sx}}\,(x, y, z, \lambda)|^2 + |P_{\mathrm{sy}}\,(x, y, z, \lambda)|^2 + |P_{\mathrm{sz}}\,(x, y, z, \lambda)|^2} \tag{2.4}$$

$$\begin{cases} P_{\mathrm{sx}}\,(x, y, z, \lambda) = \frac{1}{2} Real\,(E_y H_z^* - E_z H_y^*) \\ P_{\mathrm{sy}}\,(x, y, z, \lambda) = \frac{1}{2} Real\,(E_z H_x^* - E_x H_z^*) \\ P_{\mathrm{sz}}\,(x, y, z, \lambda) = \frac{1}{2} Real\,(E_x H_y^* - E_y H_x^*) \end{cases} \tag{2.5}$$

where α (= $4\pi\kappa/\lambda$), κ, $\Phi_{\mathrm{AM1.5}}$, P_{s}, and E/H are the extinction coefficient, imaginary part of refractive index, the spectral flux under normal AM1.5G condition, power flow, electric/magnetic field, respectively; '*Real*' and '*' are the operators. The spatial-dependent generation (G):

$$G\,(x, y, z) = \int_{\lambda_{\min}}^{\lambda_{\max}} g\,(x, y, z, \lambda)\,\mathrm{d}\lambda \tag{2.6}$$

$\lambda_{\min}$ ($\lambda_{\max}$) is the minimum (maximum) value of the absorption wavelength. Moreover, the photocurrent-density (J_{ph}) can be expressed:[73]

$$J_{\mathrm{ph}} = \int_{300\,nm}^{800\,nm} \frac{q\lambda}{hc} \Phi_{AM1.5}(\lambda) Abs(\lambda) d\lambda \tag{2.7}$$

where q, c, and h are the charge of an electron, speed of light in vacuum, and Plank constant, respectively.

2.1.2 Electrical Model

Based on the carrier generation obtained from the optical simulation, electrical simulation was conducted using the principles of carrier continuity, drift-diffusion, and Poisson's equations. These equations are presented below:[97]

$$\nabla \cdot (-\varepsilon_r \nabla V) = q(p - n + N_{\mathrm{d}} - N_{\mathrm{a}} + n_t^+ - n_t^-) \tag{2.8}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G - R;\ \frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot J_p + G - R \tag{2.9}$$

$$J_n = qn\mu_n\xi + qD_n\nabla n;\ J_p = qp\mu_p\xi - qD_p\nabla p \tag{2.10}$$

where ε_r, V, T, k_B and $\xi = -\nabla V$ are the dielectric constant and electrostatic potential, operating temperature, Boltzmann's constant and electric field, respectively; N_d/N_a and n_t^+/n_t^- are the concentration and trap density of donors/acceptors; n/p, μ_n/μ_p, J_n/J_p and $D_n/D_p = \mu_{n,p}k_BT/q$ are the concentration of electrons/holes, mobility, current density and diffusion coefficient; the total carrier recombination rate, R, can be classified into three types of recombination mechanisms:[98]

$$R = R_{\mathrm{rad}} + R_{\mathrm{Aug}} + R_{\mathrm{SRH}} + R_{\mathrm{sur}} \tag{2.11}$$

$$\begin{cases} R_{\mathrm{rad}} = B_{\mathrm{rad}}(np - n_i^2) \\ R_{\mathrm{Aug}} = (A_n n + A_p p)(np - n_i^2) \\ R_{\mathrm{SRH}} = \frac{np - n_i^2}{\tau_p(n + n_t) + \tau_n(p + p_t)} \\ R_{\mathrm{sur}} = \frac{np - n_i^2}{(n + n_{ts})/S_n + (p + p_{ts})/S_p} \end{cases} \tag{2.12}$$

where $R_{rad}/R_{Aug}/R_{SRH}/R_{sur}$ is the recombination rate from radiative or direct/Auger/SRH (Shockley-Read-Hall)/surface components with the corresponding recombination coefficient of B_{rad}/A_n (A_p)/τ_n (τ_p)/S_n (S_p); n_t/n_{ts} and p_t/p_{ts} are the electron and hole trap states in bulk/surface region. $D_{it} = S_{n,p}/\nu_{th}/\sigma_{n,p}$, where ν_{th} is the thermal velocity, $\sigma_{n,p}$ is the relevant capture cross-section for the charge carriers, and $S_{n,p}$ is the surface recombination velocity.

2.1.3 Ion Migration

In addition to charge carriers, some photovoltaic materials such as perovskite also contain mobile ions. These movable ions can affect the photoelectrical performance of the devices. For the ion migration of PSCs, the corresponding energy diagram is illustrated as shown in **Figure 2.1**.

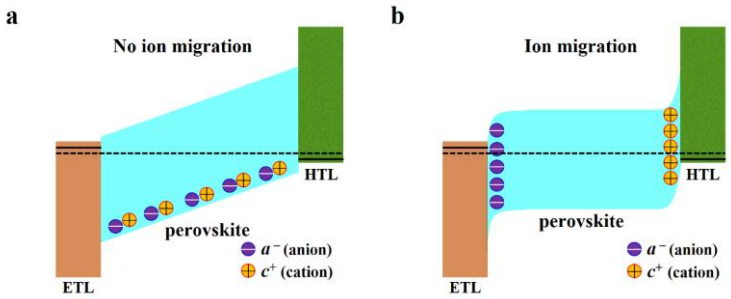

Figure 2.1 Energy band diagrams of HTL/perovskite/ETL for the cases (a)/(b) without/with ion migration.

The ion migration behavior can be replicated by integrating photoelectrical models, which are based on carrier transport equations, with ion migration models that are based on drift-diffusion equations for anions (a^-) and cations (c^+):[97]

$$J_{a^-} = qa^-\mu_{a^-}\xi + qD_{a^-}\nabla a^-;\ J_{c^+} = qc^+\mu_{c^+}\xi - qD_{c^+}\nabla c^+ \qquad (2.13)$$

where J_{a^-}/J_{c^+}, μ_{a^-}/μ_{c^+} and D_{a^-}/D_{c^+} are the current density, mobility and diffusion coefficient of anions/cations. The continuity equations used for ions:

$$\frac{\partial a^-}{\partial t} = \frac{1}{q}\nabla \cdot J_{a^-};\ \frac{\partial c^+}{\partial t} = -\frac{1}{q}\nabla \cdot J_{c^+} \qquad (2.14)$$

Poisson's equation in Eq. 2.8 was modified by:

$$\nabla \cdot (-\varepsilon_r \nabla V) = \rho = q(p - n + N_{\mathrm{d}} - N_{\mathrm{a}} + n_t^+ - n_t^- + c^+ - a^-) \qquad (2.15)$$

where ρ is the space charge density. A neutral charge inside the whole region of perovskite layer is considered:

$$\frac{1}{S}\iint a^-(x,y)dxdy = \frac{1}{S}\iint c^+(x,y)dxdy = N_i \qquad (2.16)$$

where N_i and S is the average ion concentration and the effective area of interest, respectively. Based on the above equations, the transport characteristics of free carriers and movable ions can be synchronously simulated. This is used to perform simulations to generate Figures 5.30-5.33 in chapter 5.

2.1.4 Photon Recycling

As is well known, radiative recombination, particularly in semiconductors with direct bandgaps, is an energy loss process that holds significance. Radiative recombination typically converts energy into photons, which can further generate new electron-hole pairs within the device. This phenomenon allows for the recycling or re-utilization of photons, a process commonly referred to as photon recycling (PR). Typically, photons resulting from radiative recombination can be categorized into three groups, as illustrated in **Figure 2.2**: 1) photons that escape from the device surface, 2) photons that are absorbed by the substrate, and 3) photons that are reabsorbed by the perovskite layer, leading to the generation of new electron-hole pairs. The probabilities of escape (P_e), absorption by the substrate (P_a), and reabsorption by the perovskite layer (P_r) are assigned to each case.[99,100] In cases 1 and 2, photons either escape or are absorbed parasitically, respectively, and cannot be reused to excite new electron-hole pairs.

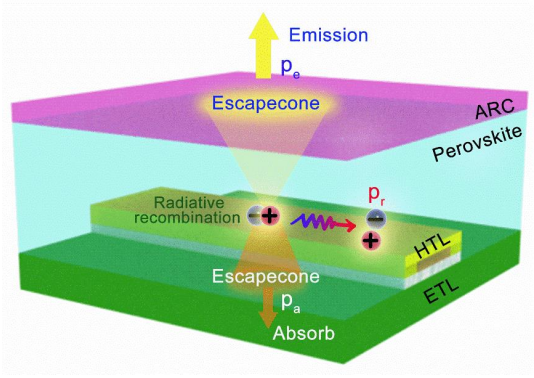

Figure 2.2 Schematic diagram of photon recycling for a perovskite device.

In terms of the perovskite IBC system, the escape probability of interested regions can

be calculated by:[99]

$$P_{\mathrm{e\_ETL}} = \frac{\int_{E_g}^{\infty} {n_{\mathrm{ARC}}}^2 A_{\mathrm{front}}(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E}{\int_{E_g}^{\infty} 4{n_{\mathrm{per}}}^2 d_{\mathrm{ETL}} \alpha(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E};\ P_{\mathrm{e\_HTL}} = \frac{\int_{E_g}^{\infty} {n_{\mathrm{ARC}}}^2 A_{\mathrm{front}}(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E}{\int_{E_g}^{\infty} 4{n_{\mathrm{per}}}^2 d_{\mathrm{HTL}} \alpha(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E} \tag{2.17}$$

Where E_g is bandgap; n_{ARC} (n_{per}) is the reflective indexes of ARC (perovskite) layer; A_{front} is the effective absorption efficiency from front-side irradiation; d_{HTL}/d_{ETL} is the thickness of perovskite layer upon HTL/ETL section, blackbody radiation flux (φ_{bb}):

$$\varphi_{\mathrm{bb}}(E) = \frac{2E^2}{h^3 c^2} \frac{1}{\mathrm{e}^{E/(k_{\mathrm{B}}T)} - 1} \tag{2.18}$$

Similar to P_{e}, P_{a} can be calculated by the following equations:

$$P_{\mathrm{a\_ETL}} = \frac{\int_{E_g}^{\infty} {n_{\mathrm{ETL}}}^2 A_{\mathrm{rear}}(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E}{\int_{E_g}^{\infty} 4{n_{\mathrm{per}}}^2 d_{\mathrm{ETL}} \alpha(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E};\ P_{\mathrm{a\_HTL}} = \frac{\int_{E_g}^{\infty} {n_{\mathrm{HTL}}}^2 A_{\mathrm{rear}}(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E}{\int_{E_g}^{\infty} 4{n_{\mathrm{per}}}^2 d_{\mathrm{HTL}} \alpha(E)\, \varphi_{\mathrm{bb}}(E)\, \mathrm{d}E} \tag{2.19}$$

where n_{ETL} (n_{HTL}) is the ETL (HTL) reflective indexes, A_{rear} the effective absorption efficiency from rear-side irradiation. By weighting the pitch size of ETL and HTL, P_{e} and P_{a} can be rewritten as:

$$P_{\mathrm{e}} = \frac{W_{\mathrm{ETL}}}{Pitch} P_{\mathrm{e\_ETL}} + \frac{W_{\mathrm{HTL}}}{Pitch} P_{\mathrm{e\_HTL}};\ P_{\mathrm{a}} = \frac{W_{\mathrm{ETL}}}{Pitch} P_{\mathrm{a\_ETL}} + \frac{W_{\mathrm{HTL}}}{Pitch} P_{\mathrm{a\_HTL}} \tag{2.20}$$

Thus, P_{r} can be deduced by:

$$P_{\mathrm{r}} = 1 - P_{\mathrm{e}} - P_{\mathrm{a}} \tag{2.21}$$

This is used to perform simulations to generate Figures 5.34-5.36 in chapter 5.

2.2 Passivation and Contact Properties

As crucial electrical parameters for predicting the properties of solar cells (SCs), passivation and contact properties require thorough investigation. These properties can be evaluated using the figure of merit for passivation and contact selectivity, denoted as:[101,102]

$$S = \log_{10}\left(\frac{k_B T}{q\rho_c J_0}\right) \tag{2.22}$$

Where ρ_c is specific contact resistance, and J_0 is recombination current. From this equation, it can be observed that a high S value ensures a simultaneous reduction in J_0 and a low ρ_c. This is used to perform simulations to generate Figure 4.20 in chapter 4.

2.2.1 Passivation Properties

In the case of c-Si SCs, passivation properties can be tested using the implied open-circuit voltage (iV_{oc}) measurement, which determines the excess minority carrier charge concentration (Δn) through quasi-steady-state photoconductance (QSSPC) measurement:[103]

$$iV_{oc} = \frac{kT}{q} In\left[\frac{\Delta n(N_d+\Delta n)}{n_i^2}\right] \tag{2.23}$$

N_d, W_{Si} and n_i is the doped concentration, thickness and intrinsic concentration of Si substrates, respectively. The effective lifetime (τ_{eff}) accounts for recombination at both the bulk and surfaces:[104]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + (J_{0,front} + J_{0,rear})\frac{(N_d+\Delta n)}{qWn_i^2} \tag{2.24}$$

If the tested devices are symmetrical structures, J_0 can be simplified:

$$J_0 = \frac{qW_{Si}n_i^2}{2(N_d+\Delta n)}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_b}\right) \tag{2.25}$$

where τ_b is the bulk recombination lifetime.

$$\frac{1}{\tau_b} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \tag{2.26}$$

$$\begin{cases} \tau_{rad} = \frac{\Delta n_{av}}{\frac{1}{W_{Si}}\int_0^{W_{Si}} R_{rad}(x)dx}; \quad R_{rad}(x) = B_{rad}\,[n(x)p(x) - n_i^2] \\ \tau_{Aug} = \frac{\Delta n_{av}}{\frac{1}{W_{Si}}\int_0^{W_{Si}} R_{Aug}(x)dx}; \quad R_{Aug}(x) = [A_n n(x) + A_p p(x)][n(x)p(x) - n_i^2] \\ \tau_{SRH} = \frac{\Delta n_{av}}{\frac{1}{W_{Si}}\int_0^{W_{Si}} R_{SRH}(x)dx}; \quad R_{SRH}(x) = \frac{n(x)\,p(x) - n_i^2}{\tau_p[n(x) + n_t] + \tau_n\,[p(x) + p_t]} \end{cases} \tag{2.27}$$

$$\Delta n_{av} = \frac{1}{W_{Si}}\int_0^{W_{Si}} \Delta n(x)dx \tag{2.28}$$

where Δn_{av} is the average excess carrier density. This is used to perform simulations to generate Figures 4.16-4.20 in chapter 4.

The physical model that considers pinholes and tunneling processes is employed to evaluate the contact properties of the device. Carrier transport occurs concurrently through two mechanisms: direct tunneling and pinhole transport. In this process, direct tunneling primarily takes place through the silicon oxide film region, while direct carrier transport predominantly occurs through the pinhole region. The transport currents of a SC include four components: $J_{maj,pin}$ ($J_{min,pin}$) and $J_{maj,tun}$ ($J_{min,tun}$) through the pinhole and SiO_x tunneling for majority (minority) carriers. According to the Fischer model, the total recombination current (J_0) can be calculated as follows:[105,106]

$$J_0 = Dn_0\,[(\frac{R_s}{\rho} + \frac{D}{f\,S_{pin}})^{-1} + (\frac{\widetilde{R}_s}{\rho} + \frac{D}{(1-f)\,S_{tun}})^{-1}] \tag{2.29}$$

$$R_s = p^2\frac{\rho}{2\pi W_{pin}}\arctan(\frac{2W}{W_{pin}}) + \rho W\,[1 - \exp(-\frac{W}{p})];\ \widetilde{R}_s = [\frac{1}{\rho W} - \frac{2\pi W_{pin}}{\rho\,p^2\arctan(\frac{2W}{W_{pin}})\exp(\frac{W}{p})}]^{-1} \tag{2.30}$$

where D is the minority carrier diffusion constant, ρ is the c-Si resistivity, $f = \pi W_{pin}^2 D_{pin}$ is the area fraction of pinholes, $R_s/\widetilde{R}_s$ is the spreading resistances across pinhole/SiO_x, $S_{pin} = J_{min,pin}/q\Delta n$ and $S_{tun} = J_{min,tun}/q\Delta n$ are the surface recombination velocities of pinhole and oxide, respectively, W is the in-diffused width, and P ($=1/\sqrt{D_{pin}}$) is the average distance of two adjacent pinholes.

For SiO_x tunneling, a direct quantum tunneling model was used. By taking into account

carrier statistics and integrating over lateral energy, the tunneling current can be expressed:

$$J = \frac{qkTm_{\text{eff}}}{2\pi^2\hbar^3} \int T(E)\, ln \left\{ \frac{1+\exp\left[\frac{E_{Fr}-E}{kT}\right]}{1+\exp\left[\frac{E_{Fl}-E}{kT}\right]} \right\} dE \qquad (2.31)$$

where m_{eff} is the effective mass, E_{fl} and E_{fr} are the quasi-Fermi levels on either side of the barrier. The transmission probability, $T(E)$, of an electron or hole through the potential barrier was calculated using Wentzel-Kramers-Brillouin (WKB) approximation. This is used to perform simulations to generate Figure 4.20 in chapter 4.

2.2.2 Specific Contact Resistivities

Contact resistivity, which significantly affects the fill factor (*FF*) and efficiency of a solar cell (SC), is of utmost importance. Two effective approaches for evaluating contact resistivities are the transfer length method (TLM)[107-113] and the Cox and Strack method (CSM).[114,115] The former is typically used for *n*-Si/HTL contacts, while the latter is employed for *n*-Si/ETL contacts.

The total contact resistance (ρ_c) with pinholes can be approximated by equation:[116]

$$\rho_c = [\frac{1}{\rho_{c,pin}} + \frac{1}{\rho_{c,tun}}]^{-1} \qquad (2.32)$$

in which $\rho_{c,pin} = R_s$ is the contact resistance through pinhole part, $\rho_{c,tun}$ is the contact resistance through SiO_x part, which can be calculated by the semiconductor-insulator-metal (MIS) model. When calculating the contact resistance, it is possible to neglect the contribution of minority carriers that have a minor effect on the total currents. The contact resistance is determined using a classical direct-tunneling model as shown in equation:[117]

$$\rho_{c,tun} = \frac{nk_B}{q A^* T P_t} \exp(\frac{q\Delta\varphi_s}{k_B T}); \quad P_t = \exp(-t_{ox}\sqrt{\frac{8qm_t}{\hbar^2}\Delta\varphi_e}) \qquad (2.33)$$

where A^*, T, m_t, P_t, t_{ox}, n, $\Delta\varphi_s$ and $\Delta\varphi_e$ are the effective Richardson constant, temperature, tunneling mass, tunneling probability, oxide thickness, ideal factor, barrier difference and tunneling barrier height, respectively. This is used to perform simulations to generate Figures 4.16-4.20 in chapter 4.

2.3 Thermal Stress

This section aims to use finite element method to solve the stress distribution inside the thin film under different annealing temperatures. To support and validate the conclusions drawn, a theoretical model was developed to investigate the relationship between deformation and thermal stress by incorporating the following governing equation[118]:

$$\rho \frac{\partial^2 \boldsymbol{u}}{\partial t^2} = \boldsymbol{E}\,(\nabla)\boldsymbol{\sigma} + \boldsymbol{f} \tag{2.34}$$

where u is the displacement field, ρ is the material density, σ is the stress, f is the volume force. Here, i only consider the thermal expansion stress and ignore the influence of other possible factors. The thermal strain tensor (ε_{th}) can be expressed as follow[119]:

$$\varepsilon_{th} = \alpha(T)\,(T - T_{ref}) \tag{2.35}$$

where $\alpha(T)$ is the temperature-dependent thermal expansion coefficient, T_{ref} is the reference temperature, which was fixed at 25°C in this study. The study utilized the COMSOL Multiphysics software with the Solid module to solve for the volume and stress distribution at different temperatures. This is used to perform simulations to generate Figures 4.13-4.14 in chapter 4.

Chapter 3 Si-Based IBC Solar Cells

3.1 Synopsis

For single crystalline silicon (c-Si) solar cells, the integration of IBC structures with high-quality heterojunction (HJ) designs has led to impressive efficiencies, with a high value of 26.7% for IBC-HJ SCs. These designs utilize IBC structures to reduce front shadowing losses and employ intrinsic/doped hydrogenated amorphous silicon [a-Si(*i*):H/a-Si(p^+) or a-Si(n^+)] stacks for the HJ region.[4] However, the incorporation of IBC structures and high-level a-Si:H films results in complex fabrication processes and increased costs, hindering the industrial implementation of high-efficiency c-Si IBC solar cells. Therefore, it is crucial to develop high-efficiency c-Si solar cells that can be fabricated using simpler integration processes.

To address this challenge, dopant-free contacts that can be easily realized through low-temperature processes or solution-based spin-coating techniques have been extensively explored. Various functional materials have been adopted for this purpose. High work-function hole transport layer (HTL) materials, such as PEDOT:PSS[28] and TMOs (*e.g.*, MoO_x[16,37], VO_x[39,40] and WO_x[38]), have been investigated. Similarly, low work-function electron transport layer (ETL) materials including metal oxides [*e.g.*, tantalum oxide (TaO_x)[120], magnesium oxide (MgO_x)[121], and titanium oxide (TiO_x)[46]], alkaline salts [*e.g.*, magnesium fluoride (MgF_x)[33], and lithium fluoride (LiF_x)[16,37]] and metals [*e.g.*, magnesium (Mg)[122], and calcium (Ca)[123]], have been studied. By incorporating high-level a-Si(*i*):H passivation layers along with MoO_x HTL and TiO_x/LiF ETL, dopant-free asymmetric hetero-contact c-Si solar cells achieved an efficiency of 20.7%.[34] Furthermore, Si-based IBC solar cells with a-Si(*i*):H/MoO_x dopant-free HTL and a-Si(*i*):H/MgF_x dopant-free ETL demonstrated an efficiency of 22.2% and a high J_{sc} of 41.5 mA/cm^2.[28] While the aforementioned achievements rely on the high-level a-Si(*i*):H passivation layers to improve interface passivation, alternative designs that

avoid using a-Si(*i*):H have also been explored. For example, Masmitjà *et al.* reported an efficiency exceeding 19% for IBC solar cells by depositing Al_2O_3/TiO_2 ETL and VO_x HTL.[34] Additionally, Lin *et al.* achieved a 16.3% efficiency for IBC solar cells by employing a PEDOT:PSS HTL and MgO_x ETL.[47]

Despite the impressive achievements in high-efficiency c-Si SCs, dopant-free SCs still have significant room for improvement. In the HJ design, there is an expectation to surpass the limitations of traditional homojunction structures and achieve exceptional open-circuit voltage (V_{oc}) and high efficiency. In addition to optimizing passivation quality in the perovskite/ETL and perovskite/HTL interfaces, the front-side of the solar cell, which does not need to collect charge carriers, plays a crucial role in separating electron-hole pairs and suppressing recombination losses. Therefore, effective passivation of the front surface is also a key consideration. One common method used for passivating the front surface of IBC solar cells involves introducing a front-surface field (FSF) formed by a heavily-doped n^+-Si or p^+-Si. This approach reduces the concentration of minority carriers and mitigates surface recombination losses to some extent. However, the heavily-doped Si layer introduces a high defect density (D_{it}) at both the n^+-Si or p^+-Si layer and the related interfaces, leading to increased surface recombination. Furthermore, the high-temperature steps required to fabricate the n^+-Si or p^+-Si layer contribute to the overall heat budget. Therefore, achieving high-efficiency IBC solar cells while maintaining a low cost through a simple fabrication process is of great significance. Another commonly-used method involves the implementation of a high-quality a-Si:H(*i*) passivation layer, which effectively reduces D_{it} to a very low value ($< 10^{10}$ $eV^{-1}cm^{-2}$).[124] In this design, a-Si:H(*i*) provides superior chemical passivation rather than relying solely on electric-field passivation.[4] However, compared to other high-efficiency c-Si technologies such as TOPCon,[53] heterojunction with an intrinsic thin-layer (HIT) devices typically exhibit a relatively low J_{sc}.[125]

Dielectric passivating films have found widespread use in Si-based IBC solar cells due to their ability to provide moderate- to high-level chemical passivation through the

dielectric layers and the electric-field effect induced by the inherent charges in those layers. This approach has been considered effective in achieving high-efficiency solar cells. For example, Savin *et al.* proposed the use of ALD Al_2O_3 layers to passivate the surface of black-Si, resulting in highly efficient IBC black-Si solar cells with efficiencies exceeding 22%. The Al_2O_3 thin films with negative built-in charges create a strong field effect, reducing front-sided recombination losses.[126] Franklin *et al.* reported a remarkable efficiency of 24.4% for Si-based IBC solar cells by employing PECVD silicon nitride (SiN_x) films to passivate the front surface. The SiN_x layers with positive built-in charges provide a strong field-effect passivation.[127] In addition to the front side, passivation of the gap region is also crucial for achieving high-efficiency IBC devices. Optimization of the gap region is necessary in order to prevent direct contact between the HTL and ETL.[15] State-of-the-art passivation technologies are employed for this purpose,[16] utilizing either electric-field or chemical passivation approaches.[16–20] The commonly used passivation material for the gap region is a-Si(*i*):H, which offers high-level chemical passivation without concerns about parasitic absorption since it is placed on the rear side of the devices.[17] However, using high-quality a-Si(*i*):H films alone cannot fully suppress carrier recombination in the gap region.[21] Combining electric-field passivation induced by the inherent charges can effectively address carrier recombination. In this approach, carrier accumulation induced by the built-in electric field effectively prevents minority carriers from reaching the defect-rich surface. This method offers advantages such as a simple fabrication process and a wide range of material options. Various applications utilizing the built-in electric field from dielectric layers have been reported. For example, Yang *et al.* used a PECVD SiN_x film with positive charges ($Q_f = +10^{12}$ cm^{-2}) to passivate the rear-sided gap region, achieving an excellent power conversion efficiency (*PCE*) of 23.0% for IBC c-Si solar cells featuring a poly-Si/tunnel silicon dioxide (SiO_2) contact.[8] Lin *et al.* proposed ALD Al_2O_3 films with negative charges ($Q_f = -4\times10^{12}$ cm^{-2}) to passivate the gap region, resulting in a 16.3% efficiency for a dopant-free IBC-HJ solar cell.[18] It would be even better if dielectric films such as thermally grown SiO_2, with a low D_{it} of 10^{10} $eV^{-1}cm^{-2}$ and a positive polarity Q_f of 10^{11} cm^{-2}, could provide

both high-level chemical passivation and electric-field effect.[22] To achieve this goal, an ALD tantalum oxide film covered by a PECVD SiN_x layer was proposed by Wan *et al.* proposed the use of an ALD tantalum oxide film covered by a PECVD SiN_x layer to passivate the Si substrates. This approach achieved a high-level to passivate the Si substrates, achieving a high-level Q_f (approximately -10^{12} cm^{-2}) and a low-level D_{it} (approximately 10^{11} $eV^{-1}cm^{-2}$).[23]

Despite numerous attempts, there is still a lack of in-depth understanding of the application of dielectric layers with charges and chemical passivation in IBC-HJ solar cells. Therefore, it is important to develop theoretical models to clarify the relationship between carrier transport, recombination, collection, and electrical parameters. Additionally, the passivation mechanism of using built-in charges should be further investigated and revealed. In this chapter, design principles of Si-based IBC solar cells with dopant-free manner are given. In addition, the passivation design by the inherent charges of dielectric films in the front-side and gap-region is proposed.

In this section, I will delve into the intricacies of designing dopant-free silicon-based IBC SCs, employing a combination of meticulous numerical simulations and experimental analyses. The focal points of the investigation encompass both structural and electrical parameters. Structural considerations involve an in-depth exploration of pitch size, size ratio, while electrical parameters include the evaluation of surface passivation quality, doping concentration, and contact properties. Moreover, I will also introduce a method to passivation the IBC SCs by fixed charges in the dielectric films. The investigative approach encompasses a thorough examination of energy distributions, potential, internal electrical fields, charge-carrier concentration, and carrier density. Through this comprehensive analysis, the aim is to provide a profound understanding of the passivation process in IBC SCs.

3.2 Dopant-Free IBC c-Si Solar Cells

This subsection introduces the design principles and carriers' transport/recombination mechanism of a double-side dopant-free IBC-HJ SC by combining experiments with simulations.

3.2.1 Simulation Details

The photoelectrical simulations were conducted for dopant-free interdigitated back contact (IBC) devices using Silvaco TCAD software. The optical simulation involved solving Maxwell's equations to determine optical properties such as optical absorption and loss. The electrical simulation involved solving drift-diffusion and Poisson's equations to obtain electrical properties including carrier concentration and potential distribution.[128,129] The carrier transport process incorporated models of concentration-dependent mobility and SRH (Shockley-Read-Hall)/Auger/radiative recombination. The simulation parameters are listed in **Table 3.1**. Other optical parameters, such as refractive index, and related electrical parameters were obtained from references by Yang *et al.*[27,130] It is important to mention that PEDOT:PSS, which is a high work-function material (> 5 eV), can be worked as the hole transport layer (HTL). For the *n*-Si/PEDOT:PSS contact, a model assuming an ideal p^+n heterojunction is considered, where the transport theory of this junction is primarily influenced by minority diffusion behaviour rather than majority-dominated thermionic emission.[131]

The schematic diagram used for both simulations and experiments is illustrated in **Figure 3.1**a. To align with the experimental results, simulations incorporated the modeling of PEDOT:PSS hole transport layer (HTL) and MoO_x electron transport layer (ETL). For the front-side design, a 60 nm-thick Si_3N_4 layer covered by a 15 nm-thick Al_2O_3 stack was employed as the passivation and anti-reflection coating (ARC) layers. Additionally, the rear-side gap region was also passivated using a high-quality Al_2O_3

film. Furthermore, measurements of minority carrier lifetimes indicated a surface recombination velocity (S_{eff}) of 300 cm/s for the PEDOT:PSS/*n*-Si interface, a S_{eff} of 620 cm/s for the MgO_x/*n*-Si interface, and a S_{eff} of 6 cm/s for the Al_2O_3/*n*-Si interface. The disparity in surface recombination velocities at the HTL/*n*-Si and ETL/*n*-Si interfaces can be attributed to two key factors. Firstly, passivation with HTL and ETL leads to a variation in the density of defect states on the silicon surface. Secondly, the asymmetric energy bands formed by HTL and ETL with *n*-Si contribute to the observed difference in the measured surface recombination velocities. Here, the measurements of minority carrier lifetimes mentioned in the statement were conducted by Dr. Lin Hao from my research group. The detailed measurement procedures and results can be found in the publication by Dr. Lin Hao.[46]

Table 3.1 Simulation parameters for dopant-free IBC SCs.

Material parameters	*n*-Si	PEDOT:PSS
Electron affinity (χ), eV	4.05	3.55
Bandgap energy, eV	1.12	1.6
Effective conduction/valence band density of states (N_c/N_v), cm^{-3}	$2.8\times10^{19}/1.04\times10^{19}$	$1\times10^{21}/1\times10^{21}$
Donor doping concentration (N_d), cm^{-3}	1×10^{15}	/
Acceptor doping concentration (N_a), cm^{-3}	/	1×10^{20}
Thickness, μm	250	0.2

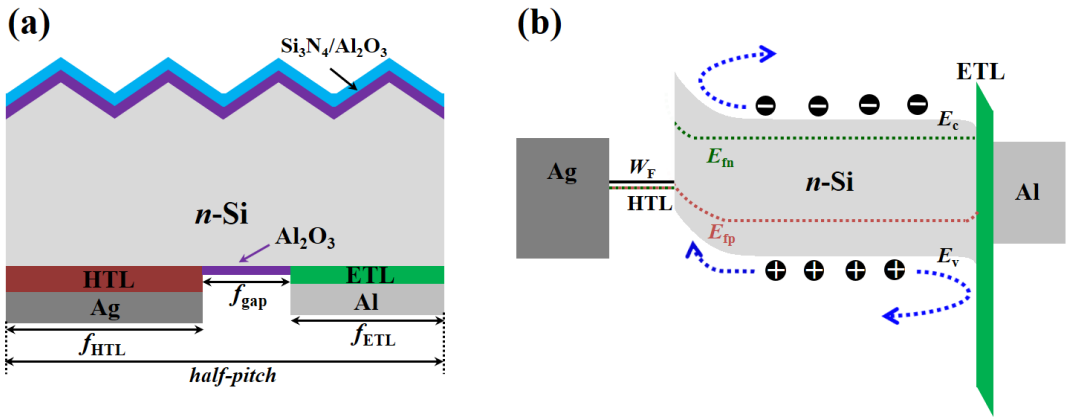

Figure 3.1 (a) Schematic diagram, and (b) the corresponding MPP-like energy band of dopant-free IBC SCs.

Moreover, **Figure 3.1**b illustrates the energy band diagram near the MPP, demonstrating a strong inversion layer in the silicon substrate due to the difference in Fermi level between the *n*-Si substrate and the work function of the PEDOT:PSS film. Here, a sufficiently high work function for HTL (low for ETL) is essential to induce a substantial band shift, leading to the creation of larger built-in voltages. This, in turn, facilitates efficiency improvements.

3.2.2 Optical and Electrical Loss Analyses

To assess the performance of these dopant-free silicon-based IBC solar cells, wavelength-dependent photoelectrical properties were simulated and presented in **Figure 3.2**. The simulations used the same parameters as the experimental ones, including a fill factor of $f_{HTL}/f_{ETL}/f_{gap}$ = 0.48/0.32/0.2, a *pitch* size of 100 μm, and a contact resistance (R_c) of 15 mΩ·cm^2.[46] It is evident from **Figure 3.2**a that, except for the ultraviolet range, the simulated external quantum efficiencies (*EQEs*) closely match the experimental results. The disparity in the electrical response between simulation and experiment in the ultraviolet range might be attributed to stronger parasitic absorption in the front Si_3N_4 layer in the experimental sample. However, since the solar spectrum in the ultraviolet band has relatively low energy, the discrepancy in response within the short wavelength range between experimental and simulation results will not have a significant impact on the overall integrated current [*i.e.*, short-circuit current density (J_{sc})].

From the optical perspective, the reflectance (*R*), transmittance (*T*), and absorptions (*Abs*) of various layers, along with their associated current density losses (J_{loss}, derived by integrating the response spectra under AM1.5G illumination conditions), namely Abs_{PEDOT}, Abs_{Si3N4}, Abs_{Al} and Abs_{Ag}, are depicted in **Figure 3.2**a, which can be quantized as follows: R = 3.18 mA/cm^2, T = 0.19 mA/cm^2, Abs_{PEDOT} = 0.48 mA/cm^2, Abs_{Si3N4} = 0.39 mA/cm^2, Abs_{Al} = 0.51 mA/cm^2, and Abs_{Ag} = 0.22 mA/cm^2. The total

optical current density loss sums up to 4.97 mA/cm^2. In general, a photocurrent density (J_{ph}) of 41.1 mA/cm^2 was achieved, considering that the incident light's current density was approximately 46.07 mA/cm^2. It should be noted that the thin electron transport layer (ETL) with minimal optical absorption (~ 1-2 nm) was disregarded in the optical simulation.

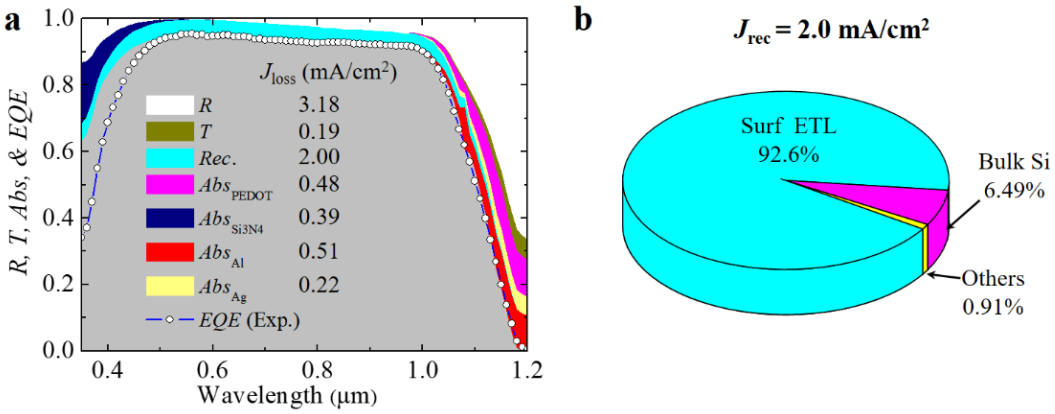

Figure 3.2 (a) Simulated photoelectrical losses for the IBC SCs featuring MoO_x HTL and MgO_x ETL. The experimental *EQE* spectra was also included. (b) Distribution of the main recombination (J_{rec}) contributions from simulation results. Here, it is important to mention that the experimental *EQE* spectrum is conducted and provided by Dr. Hao Lin in my laboratory.

Furthermore, **Figure 3.2**b illustrates the contributions of different recombination channels, represented as J_{rec}, leading to recombination losses in each section. Notably, the two primary carrier recombination channels originate from the *n*-Si/ETL interface (referred to as Surf ETL), accounting for 92.6% of the recombination proportion, and the *n*-Si substrate involving Auger and/or SRH recombination (referred to as Bulk Si), contributing 6.49% to the recombination losses. Photoelectrical loss predominantly occurs at the ETL/n-Si interface due to the higher interface recombination velocity in comparison to the HTL/n-Si interface. Other recombination channels contribute less than 1% to the J_{loss}, primarily due to the exceptional chemical passivation and/or electric-field passivation at the corresponding interfaces.

The current density-voltage (*J-V*) characteristic curves under normal AM1.5G illumination were presented in both simulations and experiments, as shown in **Figure 3.3**. The corresponding electrical performances were also displayed under the same conditions. In the simulation case, the following values were achieved: a J_{sc} of 39.1 mA/cm2, a V_{oc} of 591 mV, a fill factor (*FF*) of 80.9%, and a *PCE* of 18.7%. On the other hand, the experimental device achieved a J_{sc} of 38.4 mA/cm^2, a V_{oc} of 581 mV, an *FF* of 73.1%, and a *PCE* of 16.3%.

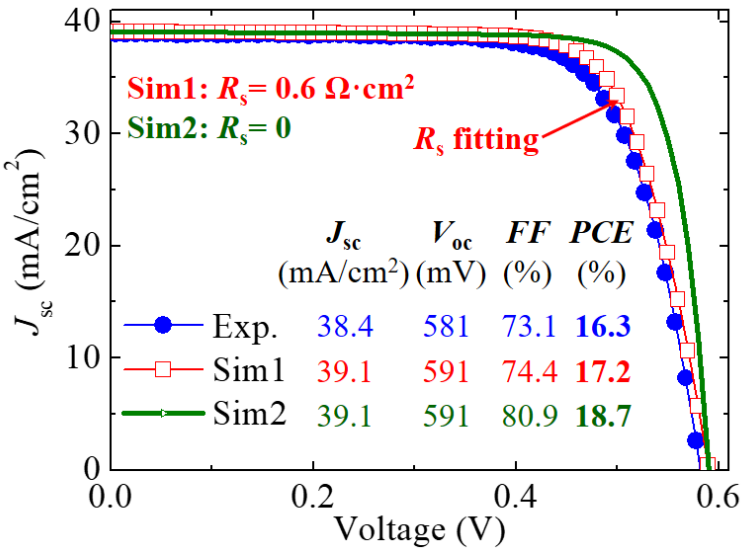

Figure 3.3 Light *J-V* curves for simulations and experiments. Here, it is important to mention that the experimental *I-V* curve is conducted and provided by Dr. Hao Lin in my laboratory.

Figure 3.3 illustrates that the difference in device efficiency between simulation and experiment primarily arises from the disparity in *FF*. To better match the experimental results, an artificial resistance (R_s) of 0.6 Ω·cm^2 was added to the simulation, as depicted in **Figure 3.3**. In reality, even the best-performing *n*-Si/PEDOT:PSS solar cells still suffer from relatively high R_s values. It is worth noting that the resulting V_{oc}, with an experimental value of 581 mV and a simulated value of 591 mV, falls significantly lower than the best V_{oc} values (> 700 mV) observed in dopant-free Si-based IBC solar cells.[36] This prompts an investigation into the reason behind this low V_{oc}, specifically focusing on the surface recombination rate at the *n*-Si/ETL interface.

It is worth mentioning that a high-quality passivation of the front-surface and rear-side gap region can be achieved using an Al_2O_3 passivation layer, which possesses an inherent negative charge density of -4×10^{12} cm^{-2} and a low S_{eff} of 6 cm/s.[132] Such excellent passivation meets the requirements for fabricating IBC-HJ solar cells with high efficiencies.[124]

3.2.3 Structure Optimization

Given the confirmed impact of the ETL interface on device performance, it is crucial to investigate the influence of *pitch* size, and passivation quality of ETL/*n*-Si interface on device efficiencies. Here, PEDOT:PSS and MoO_x were employed as the HTL and ETL, respectively. By utilizing these materials, i kept the work functions of the HTL and ETL, as well as the recombination rates of HTL/*n*-Si and ETL/*n*-Si interfaces, *i.e.*, a S_{eff} of 300 cm/s for the PEDOT:PSS/*n*-Si interface, a S_{eff} of 620 cm/s for the MgO_x/*n*-Si interface, and a high work-function of 5 eV for the PEDOT:PSS. The detailed electrical parameters can be found in **Table 3.1**. My objective was to enhance the efficiency of the device by optimizing the *pitch* size, size proportion, and recombination rate of the *n*-Si/ETL interface. The effects of *pitch* size are demonstrated in **Figure 3.4**a-**3.4**b. **Figure 3.4**a presents the *PCE* values under different f_{ETL} values and *pitch* sizes, with a fixed f_{HTL}/f_{gap} ratio of 0.48/0.2 as a control. The following observations can be made from these plots: 1) as f_{ETL} decreases from 0.6 to 0.1, the *PCE* values show an upward trend; 2) with an increase in *pitch*, the *PCE* values initially decrease smoothly and then decline more rapidly; 3) *PCE* values above 20% can only be achieved when f_{ETL} is less than 0.1 under a *pitch* of 100 μm. This indicates that optimizing the geometric structure alone, even with an unsatisfactory passivation level (*i.e.*, S_{ETL} = 620 cm/s), can boost the *PCE* to 20%.

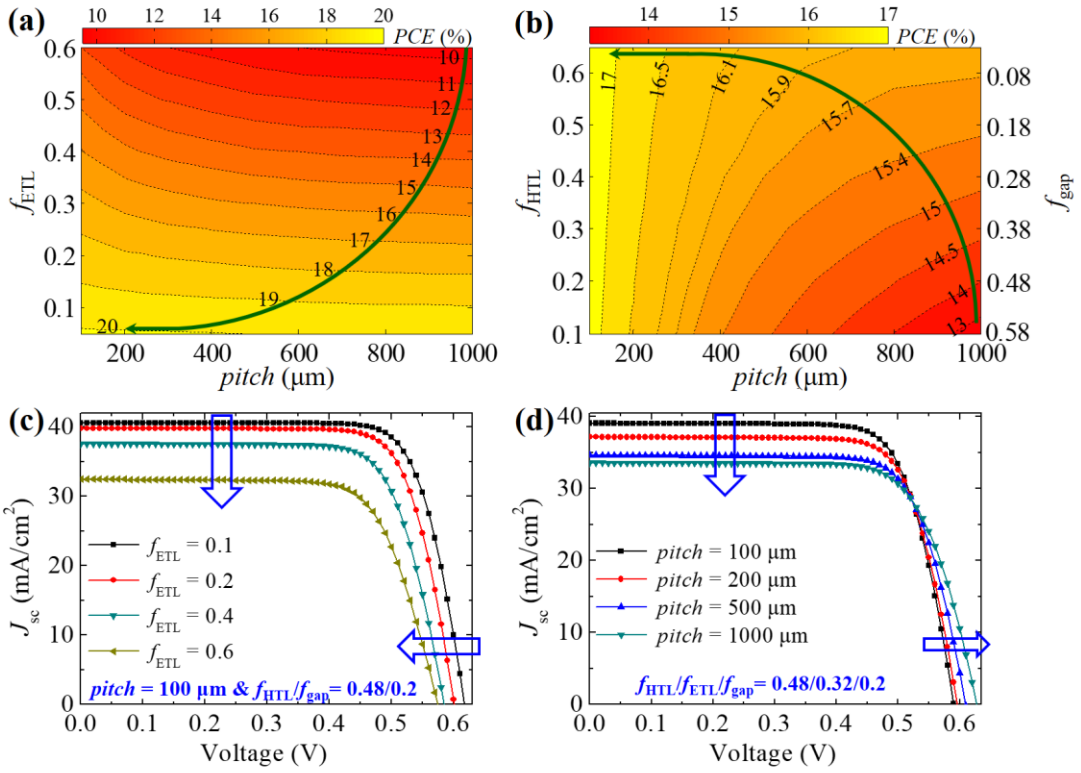

Figure 3.4 (a) *PCE* values for this kind of Si-based IBC devices as functions of *pitch* and f_{ETL} under a f_{HTL} of 0.48 and a f_{gap} of 0.2. (b) *PCE* values of this kind of Si-based IBC devices as functions of *pitch* and f_{HTL} (f_{gap}) under f_{ETL} = 0.32. (c)-(d) The corresponding *J-V* characteristic curves with the diverse f_{ETL} and *pitch*.

Furthermore, *J-V* curves were plotted in **Figure 3.4**c to illustrate the impact of diverse f_{ETL} values under a *pitch* of 100 μm and a fixed f_{HTL}/f_{gap} ratio of 0.48/0.2. As f_{ETL} increases from 0.1 to 0.6, J_{sc} and V_{oc} gradually deteriorate, resulting in a significant degradation in *PCE*. This can be easily understood: if f_{ETL} is sufficiently large, holes near the ETL region need to traverse a longer horizontal distance before being collected by HTL, increasing the probability of recombination and consequently leading to lower J_{sc}, V_{oc} and *PCE*. To optimize the f_{HTL} and f_{gap} values with a constant f_{ETL} of 0.32, **Figure 3.4**b demonstrates the following observations: 1) if f_{HTL} is larger than 0.6, the *pitch* becomes insensitive to device *PCE*; 2) when f_{HTL} is too small (approximately 0.1), *PCE* is largely dependent on the *pitch*; 3) a larger f_{HTL} and a smaller *pitch* contribute to higher performance, yielding the highest *PCE* of 17.7% under f_{HTL} = 0.65 and a *pitch*

of 100 μm. As shown in **Figure 3.4**b, when f_{HTL} decreases from 0.65 to 0.48, *PCE* only decreases by 0.4%, going from 17.7% to 17.3%. This indicates that changing f_{ETL} is a more effective way than increasing f_{HTL} to improve efficiency in small *pitches*. When the fill rate of $f_{HTL}/f_{ETL}/f_{gap}$ is fixed at 0.48/0.32/0.2, **Figure 3.4**d displays the *J-V* curves depicting the corresponding results under different *pitches*. These curves reveal a decreasing trend in J_{sc} but an increasing trend in V_{oc} as the *pitch* increases from 100 to 1000 μm.

The simulated parameters that were extracted from **Figure 3.4**d were shown in **Figure 3.5**. The experimental results presented by lines were also shown in this figure. It is not difficult to find out that: 1) J_{sc} values of experiment and simulation cases have a downward trend with the increase of *pitch* from 100 to 1000 μm; 2) V_{oc} values of experiment and simulation cases have an increasing trend, apart from experimental sample under *pitch* = 200 μm, which may be caused by unstable manufacturing processes. Meanwhile, *FF* values of the simulation case have an increasing trend with the increasing of *pitch* from 100 to 200 μm and then have a downward trend with the increasing of *pitch* from 200 to 1000 μm. It should be emphasized that the relatively low J_{sc} conducted by experiment is owing to the flat structures in the front-side of devices, resulting in the strong optical reflection losses. The deficit of V_{oc} and *FF* between simulation and experiment should be caused by the imperfect integrated process. As a result, *PCE* values of experiment and simulation cases have a downward trend with the increase of *pitch* from 100 to 1000 μm.

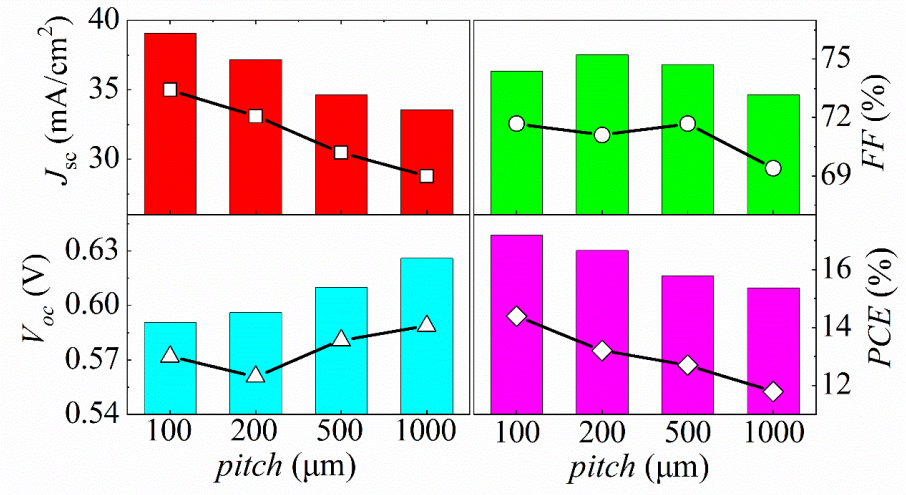

Figure 3.5 Electrical parameters including J_{sc}, V_{oc}, *FF* and *PCE* of this kind of Si-based IBC devices under the various *pitch* at a fixed $f_{HTL}/f_{ETL}/f_{gap}$ of 0.48/0.32/0.2, where the simulated and experimental results were expressed by bars and lines, respectively. Here, it is important to mention that the experimental data are conducted and provided by Dr. Hao Lin.

The results presented in **Figures 3.4** and **3.5** are based on a fixed passivation quality of the ETL/*n*-Si interface. To further investigate the impact of passivation quality on the performance of these IBC SCs, the *PCE* values were examined under varying passivation qualities, as shown in **Figure 3.6**. It can be easily found from **Figure 3.6** that: 1) for the four different *pitches*, the *PCE* values initially decrease with increasing S_{ETL} from 1 to 10^5 cm/s, and then stabilize for S_{ETL} values greater than 10^5 cm/s. This indicates that the passivation quality of the ETL/*n*-Si interface, particularly for S_{ETL} values below 10^4 cm/s, plays a crucial role in determining device efficiency; 2) when the interface passivation is of high quality, characterized by S_{ETL} values less than 10 cm/s, the *PCE* values are relatively insensitive to S_{ETL}. There is a slight decrease in *PCE* for *pitch* = 1000 μm compared to case of *pitch* = 100 μm; 3) in the range of 10 cm/s < S_{ETL} < 10^3 cm/s, smaller *pitches* offer a comparative advantage in terms of *PCE* due to higher J_{sc} values, as shown in **Figure 3.6**; 4) if S_{ETL} exceeds 10^4 cm/s, larger *pitches* are expected to achieve higher *PCE* due to larger V_{oc} values. In summary, achieving high device efficiency requires a high-quality passivation with a low S_{ETL}.

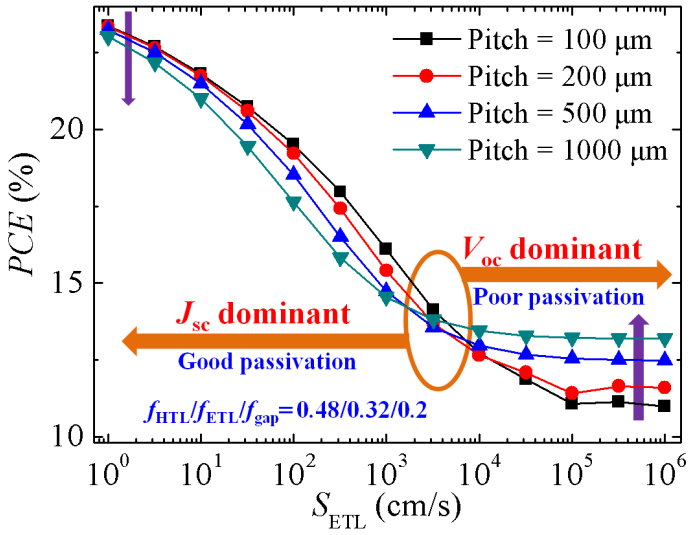

Figure 3.6 *PCE* of IBC SCs under the different S_{ETL} and *pitch*.

It is important to note that the findings presented in **Figure 3.6** are not in contradiction with those shown in **Figure 3.4**a and **3.4**b. In **Figure 3.4**a, the recombination rate of ETL/*n*-Si interface (S_{ETL}) was fixed at 620 cm/s. In this case, the smaller *pitch* is of more comparative advantage on *PCE* due to higher J_{sc} values. If S_{ETL} exceeds 10^4 cm/s, the *PCEs* of devices will be very low regardless of the *pitches* as shown in **Figure 3.6**. In this case, larger *pitches* are expected to achieve higher *PCE* due to larger V_{oc} values. This conclusion can be confirmed by the results of **Figure 3.4**d, where larger *pitches* show higher V_{oc} values than that of the smaller *pitches*.

3.2.4 Carrier Transport Mechanism

In order to gain a deeper understanding of the influence of electrical parameters, such as *pitch*, size ratio, and S_{ETL}, on device efficiencies, an analysis of the carrier transport and recombination mechanisms were conducted. This analysis involved examining the hole current density and the distribution of electric fields. The results of this analysis are presented in **Figure 3.7**. Compared to the *pitch* = 100 μm shown in **Figure 3.7**a, the hole current density is weakened near the gap/ETL interfacial region when the *pitch* is increased to 1000 μm, as shown in **Figure 3.7**b. However, the case with a *pitch* of 1000

μm exhibits a high hole current density in the region far from the gap/ETL interface, leading to strong recombination and consequently a low J_{sc} for larger *pitches*, as depicted in **Figure 3.5**. When the bias voltage (V_b) is increased to 0.55 V, the hole current densities on the ETL region are significantly enhanced for both *pitch* values of 100 μm and 1000 μm, as illustrated in **Figure 3.7**c and **3.7**d. This enhanced current density results in strong recombination under the applied bias voltage.

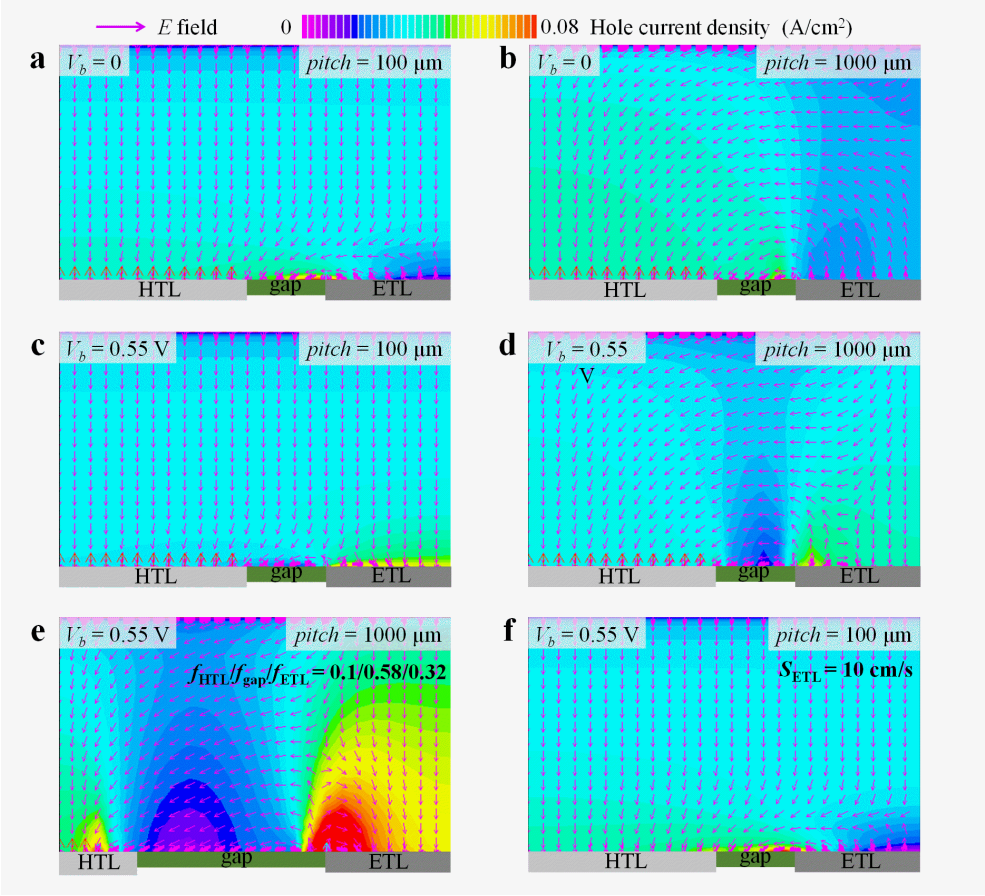

Figure 3.7 Distributions of electric field and hole current density under the different cases, including V_b = 0 for *pitch* = (a)/(b) 100/1000 μm ($f_{HTL}/f_{gap}/f_{ETL}$ = 0.48/0.2/0.32, and S_{ETL} = 620 cm/s), V_b = 0.55 V for *pitch* = (c)/(d) 100/1000 μm ($f_{HTL}/f_{gap}/f_{ETL}$ = 0.48/0.2/0.32, and S_{ETL} = 620 cm/s), (e) $f_{HTL}/f_{gap}/f_{ETL}$ = 0.1/0.58/0.32 (V_b = 0.55 V, *pitch* = 1000 μm, and S_{ETL} = 620 cm/s), and (f) S_{ETL} = 10 cm/s (V_b = 0.55 V, *pitch* = 100 μm, and $f_{HTL}/f_{gap}/f_{ETL}$ = 0.48/0.2/0.32).

Additionally, **Figure 3.7**e demonstrates that as the rear gap length increases (f_{gap} = 0.58) compared with the case in **Figure 3.7**d (f_{gap} = 0.2), the current densities of holes within

the gap-region are further amplified. Simultaneously, the horizontal *E* field, particularly in the region covered by the ETL, weakens, resulting in a degradation in performance. Compared with the case in **Figure 3.7**c (S_{ETL} = 620 cm/s), **Figure 3.7**f depicts the situation when the ETL is well-passivated (S_{ETL} = 10 cm/s). In this case, the strength of the horizontal *E* field remains intact, and the hole current density near the ETL is effectively suppressed compared to the scenario with the relatively poor interface passivation, as shown in **Figure 3.7**c. These observations highlight that the passivation quality of the ETL is crucial for achieving high device performance, even under bias voltage conditions.

3.2.5 Performance Improvement Roadmap

The aforementioned results have been obtained using a fixed doping concentration of the *n*-Si substrate ($N_d = 10^{15}$ cm^{-3}). However, it is necessary to investigate the electrical parameters under different N_d values.

Figure 3.8 presents the electrical parameters as a function of N_d, while maintaining a constant S_{ETL} of 620 cm/s. Two cases were considered: $f_{HTL}/f_{ETL}/f_{gap}$ = 0.48/0.32/0.2 and 0.8/0.1/0.1. Both cases exhibit a similar trend, but higher values are obtained for $f_{HTL}/f_{ETL}/f_{gap}$ = 0.8/0.1/0.1. For the case of $f_{HTL}/f_{ETL}/f_{gap}$ = 0.48/0.32/0.2, initially, J_{sc} linearly decreases with increasing N_d, followed by a rapid downtrend for $N_d > 1\times10^{16}$ cm^{-3}. In the case of $f_{HTL}/f_{ETL}/f_{gap}$ = 0.8/0.1/0.1, J_{sc} remains unchanged if $N_d < 10^{16}$ cm^{-3}, but it exhibits an immediate downtrend for $N_d > 10^{16}$ cm^{-3}. Moreover, V_{oc} and *FF* values for both cases initially show a linear increase and then stabilize. Consequently, the inverse trends of J_{sc} and V_{oc} or *FF* result in an initial increase and subsequent decrease in *PCE*, with the highest value of *PCE* achieved at $N_d = 2\times10^{16}$ cm^{-3}. It is important to note that in practical scenarios, the bulk lifetime and carrier mobility of c-Si substrate typically decrease as the doping concentration increases. However, in this simulation, i did not consider these variations and kept the bulk lifetime and mobility of the c-Si

substrate unchanged. As a result, the optimal doping concentration of the c-Si substrate obtained in my simulation may appear higher than expected.

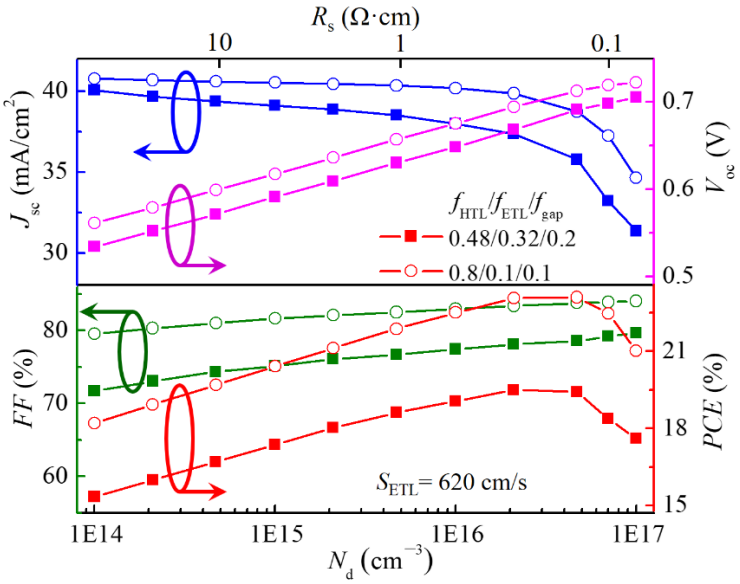

Figure 3.8 Electrical parameters including J_{sc}, V_{oc}, *FF* and *PCE* at the different N_d.

To further investigate the contact and passivation properties of Si-based IBC devices, the relationship between the device *PCE* and the effective recombination velocity (S_{ETL}) and contact resistance of ETL/Si interface (ρ_{ETL}) was examined, as illustrated in **Figure 3.9**. The optimal fill rates for the HTL, ETL, and the gap were selected as $f_{HTL}/f_{ETL}/f_{gap}$ = 0.8/0.1/0.1. In this figure, a simulated *PCE* of approximately 20.3% was achieved for the case of using a magnesium oxide (MgO_x) ETL with a S_{ETL} of 620 cm/s and an ETL contact resistance of 15 mΩ·cm^2. From **Figure 3.9**, it is evident that optimizing the passivation quality by reducing the S_{ETL} offers the best approach to achieve high efficiencies. If the S_{ETL} is less than 10 cm/s, a predicted *PCE* exceeding 24% can be expected. As a comparison, other reported ETLs, such as titanium oxide (TiO_x), magnesium fluoride (MgF_x), titanium oxide (TiO_x), and lithium fluoride (LiF), as well as their related stacks, were also indicated in **Figure 3.9**. This suggests that by replacing MgO_x with state-of-the-art ETLs based on TiO_x, a-Si:H(*i*)/MgF_x, a-Si:H(*i*)/LiF, *etc*., a *PCE* exceeding 23% can be achieved with the current device. Although the results discussed are based on the HTL/ETL combination of PEDOT:PSS/MgO_x, they have a

wide range of applicability due to the following reasons: 1) it has been confirmed that PEDOT:PSS/*n*-Si HJ (heterojunction) solar cells with a back contact design have achieved excellent device performance with a high *PCE* over 20%, indicating that the use of a PEDOT:PSS film does not pose major obstacles in pursuing high *PCE*;[133] 2) the research conducted on ETLs, related design principles, and loss mechanisms is mostly independent of the HTL materials used.

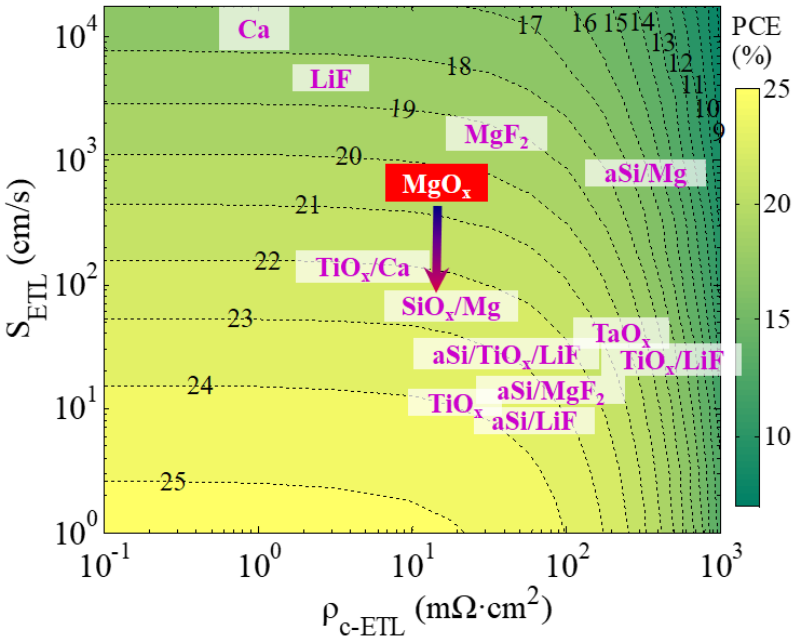

Figure 3.9 *PCE* values as functions of S_{ETL} and ρ_{c_ETL} at a fixed $f_{HTL}/f_{ETL}/f_{gap}$ of 0.8/0.1/0.1.

3.2.6 Conclusion

A completely dopant-free IBC solar cell to investigate the design principles and related mechanisms was proposed. Taking a device with a PEDOT:PSS HTL and MgO_x ETL as an example, the photoelectrical losses in each region were examined and explanations for the observed poor performance in the current design were provided. The results and optimized schemes indicated that the efficiency of dopant-free silicon-based IBC devices could be easily improved by optimizing the device pitch, area fill ratio, or reducing S_{eff} of the ETL/*n*-Si interface. The carrier transport and recombination mechanisms were clarified by examining the current density of minority carriers and

the electric field distributions in the relevant regions. The findings can be summarized as follows: 1) a device with a larger pitch is expected to achieve a low J_{sc} but a high V_{oc}; 2) increasing the proportion of the rear-gap area fill will negatively impact device performance; 3) effectively reducing recombination losses at the ETL/*n*-Si interface can significantly improve device performance. Furthermore, the impact of passivation quality and contact resistance on efficiency was demonstrated. It is predicted that an outstanding efficiency of over 24% is achievable if the ETL/*n*-Si surface is passivated with high quality, resulting in a corresponding S_{eff} of only 10 cm/s.

3.3 Front-Surface Charge Passivation

3.3.1 Simulation Details

The Silvaco TCAD software was utilized to conduct photoelectric simulations for the

IBC SCs.[128] For the simulation, a planar configuration was employed, with a Si_3N_4 (60 nm)/Al_2O_3 (15 nm) stack serving as the front-sided antireflection coating (ARC) and passivation layer.[46] The anode was made of Ag (300 nm), while the cathode was made of Al (300 nm-thick). The simulation considered a standard illumination condition using AM1.5G as the light source. The model adopted a half-pitch with symmetric boundary conditions. As for the hole transport layer (HTL), a high work-function (WF_{HTL}) of 5.2 eV was assumed. This value is sufficiently high to induce energy band bending of the Si surface.[134]

Figure 3.10a/**3.10**b depicts the schematic devices of *n*-Si SCs with IBC designs, where the front dielectric layer carries a negative or positive charge. The simulations used a planar structure on both sides and a fully dopant-free contact. The *n*-Si substrate had a doping concentration (N_d) of 2.3×10^{15} cm^{-3} with a thickness of 250 μm. The following parameters were considered: 1) the HTL employed a high work-function with a value of 5.2 eV;[134] 2) the *pitch* was maintained at 2000 μm;[36] 3) the area fill proportion of the HTL/gap/ETL layers ($f_{HTL}/f_{gap}/f_{ETL}$) was set at 0.6/0.2/0.2. The surface recombination ratios of the relevant interfaces, namely S_{HTL} of the HTL/*n*-Si interface, S_{gap} of the gap/*n*-Si interface, and S_{ETL} at the ETL/*n*-Si interface, were kept at 10 cm/s. The related electrical parameters used for this simulation was listed in **Table 3.2**.

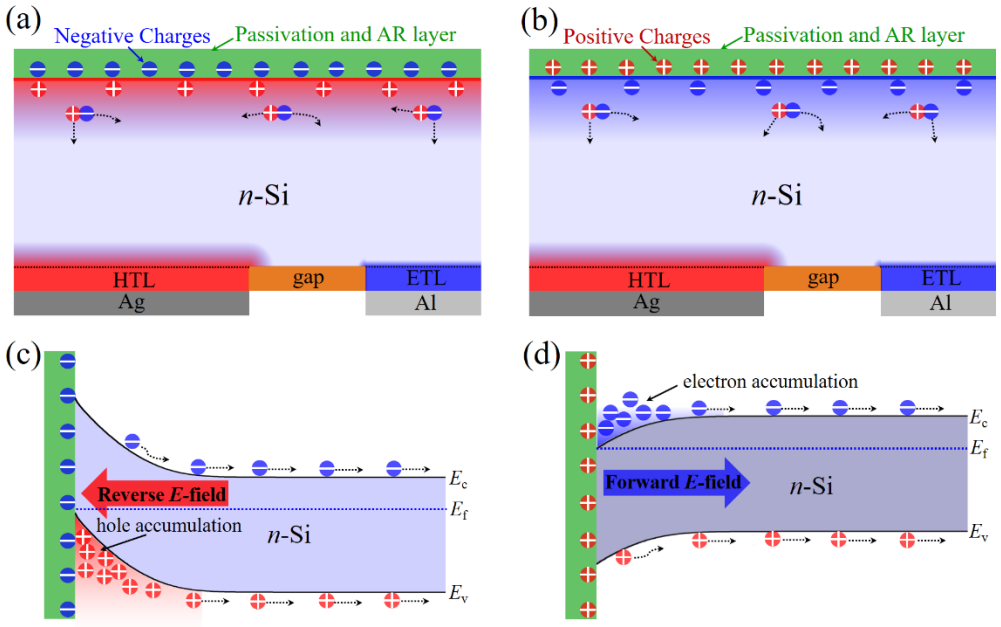

Figure 3.10 Schematic devices and the related energy bands for the cases with (a)/(c) negative and (b)/(d) positive charges.

Table 3.2 Electrical parameters for this simulation.

Parameters	Values
Donor doping concentration (N_d) of Si substrate	2.3×10^{15} cm^{-3}
Thickness of Si substate	250 μm
Lifetime of Si substrate	3 ms
Electron/hole mobility of Si substrate	1000/800 cm^2/Vs
$f_{HTL}/f_{gap}/f_{ETL}$	0.6/0.2/0.2
Pitch	2000 μm
Si_3N_4/Al_2O_3 ARC	60/15 nm
Recombination velocity of HTL/*n*-Si	10 cm/s
Recombination velocity of gap/*n*-Si	10 cm/s
Recombination velocity of ETL/*n*-Si	10 cm/s
Work function of HTL	5.2 eV

As is well known, the effective surface recombination ratio, S_{eff}, can be determined using Equation 3.1:[135]

$$S_{\text{eff}} = \frac{1}{\Delta n}\frac{n_s p_s - n_i^2}{(n_s+n_i)/S_p+(p_s+n_i)/S_n} \quad (3.1)$$

Equation 3.1 suggests two approaches to reducing recombination losses at the related surfaces: reducing the density of interface traps (D_{it}) through chemical component passivation or reducing the carrier concentration, especially for minority carriers, through electric-field passivation. In this case, electric-field induced passivation is achieved by the interface charge (Q_f) of dielectric passivation thin films (DPTFs) through the sample fabrication process. Diagrams of the corresponding energy band structures are shown in **Figure 3.10**c/**3.10**d, which reveal the accumulation of holes/electrons on the front side of the Si surface at thermal equilibrium, resulting in a reversed/forward electric field for the negative/positive case. The induced electric field on the front surface prevents bulk-Si carriers from reaching the front interface and effectively separates electron-hole pairs.

3.3.2 Passivation Effect

The relationship between the *PCE* and the D_{it} and Q_f is illustrated in **Figure 3.11**a. Upon careful observation, the following conclusions can be drawn:

1) When Q_f exceeds a value of 5×10^{12} cm^{-2}, an outstanding *PCE* (> 22%) can be achieved for both negative and positive charge cases in the planar IBC-HJ SCs.

2) In the absence or presence of a weak interface charge ($Q_f < 10^{11}$ cm^{-2}), a remarkable *PCE* can be attained with a low D_{it} value of less than 10^{10} $eV^{-1}cm^{-2}$.

3) A large Q_f demonstrates a high tolerance to D_{it} for both negative and positive charge cases.

4) The lowest *PCE*, indicated by the white line, occurs in the case of a weak negative charge ($Q_f \sim -3\times10^{10}$ cm^{-2}) rather than in the absence of interface charge. The state-of-the-art alternative DPTFs are highlighted, suggesting that excellent *PCEs* can be achieved using various DPTFs such as ALD Al_2O_3, tantalum oxide (TaO_x), and thermally grown SiO_2.[132,135]

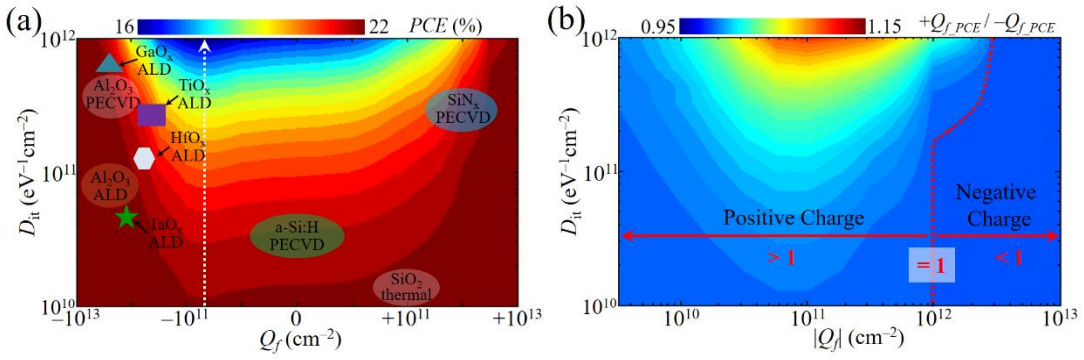

Figure 3.11 (a) *PCE* values, and (b) *PCE* proportions of devices of positive/negative charges as functions of D_{it} and Q_f. In this simulation, defects are introduced at the front interface of *n*-Si, while charges are distributed within the dielectric passivation thin films.

To provide a more straightforward comparison between the two polar charges, **Figure 3.11**b presents the *PCE* ratio (the efficiency ratio is calculated by dividing the efficiency

under positive charge by the efficiency under an equal negative charge, *i.e.*, PCE_{+Qf}/PCE_{-Qf}). The following observations can be made from **Figure 3.11**b: 1) when D_{it} is less than 2×10^{11} $eV^{-1}cm^{-2}$, devices with a high negative charge ($Q_f > 10^{12}$ cm^{-2}) exhibit higher performance compared to the devices with the equal positive charge. This conclusion is supported by observation that the ratio PCE_{+Qf}/PCE_{-Qf} is less than 1 when D_{it} is less than 2×10^{11} $eV^{-1}cm^{-2}$; 2) when D_{it} exceeds 5×10^{11} $eV^{-1}cm^{-2}$, devices with a positive charge have an advantage over the negative charge case until Q_f reaches 3×10^{12} cm^{-2}; 3) as D_{it} increases from 10^{10} $eV^{-1}cm^{-2}$ to 10^{12} $eV^{-1}cm^{-2}$, a bell-shaped contour is observed, with the minimum values occurring at $Q_f = 10^{11}$ cm^{-2}. These observations highlight the importance of both D_{it} and Q_f in determining the optimal charge polarity for achieving higher *PCE* values. The specific values of D_{it}, Q_f, and their interplay have an impact on the overall device performance.

Furthermore, the performance of the IBC-HJ SCs was evaluated for various *pitches*, as presented in **Figure 3.12**a. For comparison, the traditional front surface field (FSF) design with heavily-doped Si configuration was also considered. The results indicate the following:

1) As the half-pitch increases from 100 to 1500 μm, the *PCEs* remain stable for the low D_{it} (3×10^{10} $eV^{-1}cm^{-2}$), moderate D_{it} (3×10^{11} $eV^{-1}cm^{-2}$) with high negative Q_f (-4×10^{12} cm^{-2}), and FSF cases. However, the *PCEs* for the moderate (3×10^{11} $eV^{-1}cm^{-2}$) and high (10^{12} $eV^{-1}cm^{-2}$) D_{it} cases show dependence on the *pitch*.

2) The *J-V* characteristic curves of the relevant cases at a *pitch* of 2000 μm are depicted in **Figure 3.12**b. It is evident that the moderate and high D_{it} cases with $Q_f = 0$ exhibit relatively low electrical parameters (J_{sc} and V_{oc}). Additionally, a slight reduction in J_{sc} and V_{oc} is observed for the low D_{it} and FSF cases compared to the moderate D_{it} case with high negative Q_f. This reduction is attributed to carrier recombination at the front surface. These findings suggest that a combination of chemical passivation (low D_{it}) and field-electric passivation (high Q_f) is the most effective approach to suppress front-surface carrier recombination and achieve high *PCE*.

These results emphasize the importance of optimizing both chemical and field-

electric passivation strategies to enhance the overall performance of IBC-HJ SCs, particularly in mitigating front-surface carrier recombination.

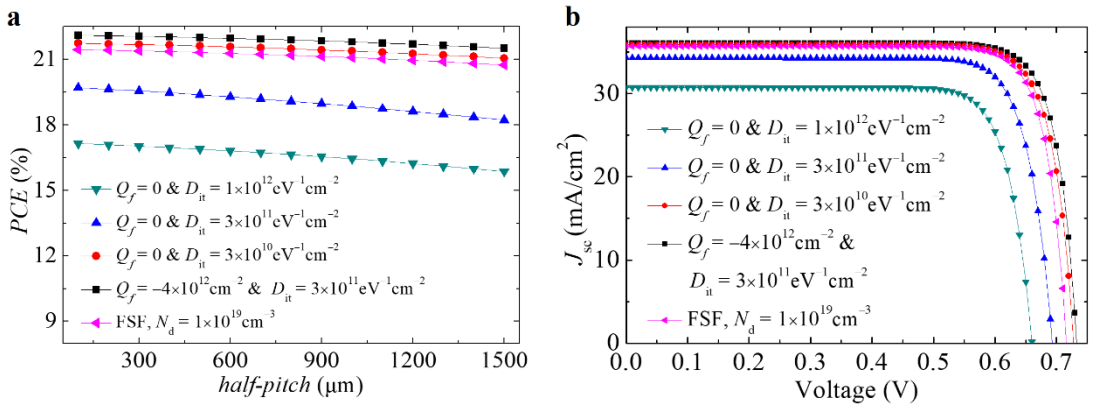

Figure 3.12 (a) *PCE* values of the related devices as a function of *half-pitch* for different cases, where the traditional FSF with heavily-doped Si was also taken into account. (b) *J-V* curves with *pitch* = 2000 μm for different cases. Here, D_{it} = 3×10^{11} eV^{-1}cm^{-2} and Q_f = –4×10^{12} cm^{-2} are considered since they closely resemble the values typically associated with PECVD Al_2O_3.

To support the aforementioned conclusions, **Figure 3.13** illustrates the distributions of energy band, potential, electric-field strength, and carrier concentration proportion. The following information can be observed from the figure:

1) Energy level Distributions: **Figure 3.13**a shows the energy level distributions for the discussed cases under AM1.5 illumination. In contrast to the case with Q_f = 0, which exhibits an almost flat energy band, the conduction energy band (E_c) for the negative/positive charge cases deviates from/closes to the Fermi level (E_f) of the Si substrate. The extent of deviation or closure depends on the quantity of the charge for both negative and positive charge cases.

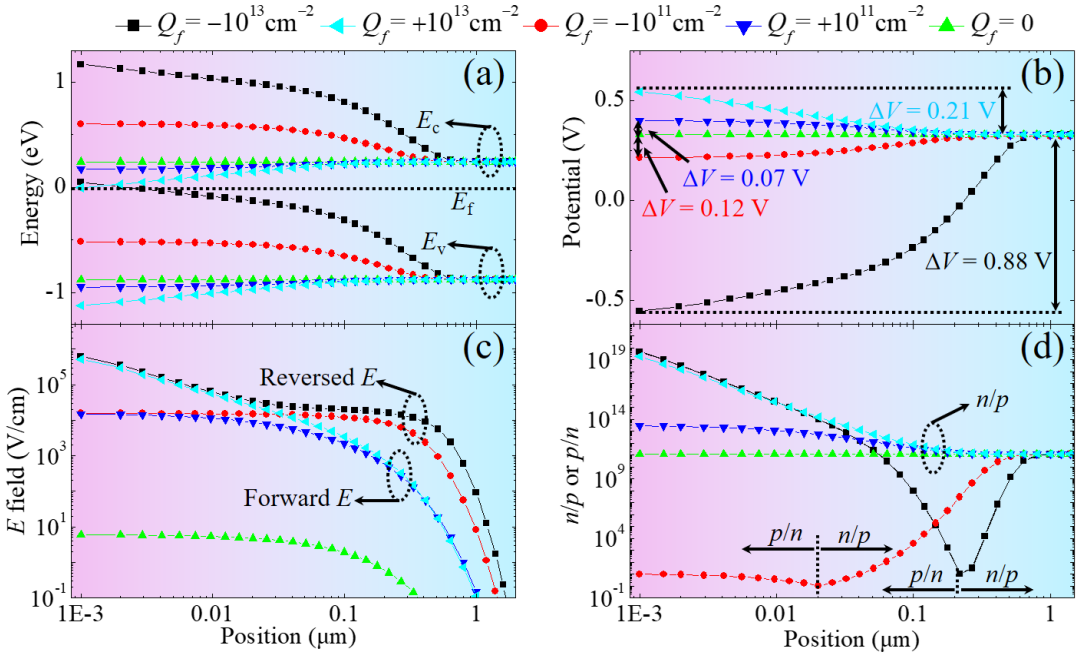

Figure 3.13 Cross-sectional distributions of (a) energy level, (b) potential, (c) electric-field, and (c) carrier concentration proportion at vertical direction under dark condition.

2) Potential Distributions: **Figure 3.13**b displays the potential distributions. In the case with no charge, the potential near the front surface remains relatively unchanged. The maximum potential differences (ΔV) at the front surface for Q_f = -10^{13}/-10^{11}/$+10^{11}$/$+10^{13}$ cm^{-2} are measured as 0.29/0.12/0.05/0.2 V, respectively.

3) Electric-Field Strength: The electric-field strength near the front surface is shown in **Figure 3.13**c. It indicates the magnitude of the electric field in that region.

4) Carrier Concentration Ratio: **Figure 3.13**d presents the carrier concentration ratio, which represents the quality of surface passivation. A higher value indicates better surface passivation quality and lower recombination. The ratio is defined as the proportion of majority carrier concentration (n/p or p/n) at the front surface.

These analyses of energy band, potential, electric-field strength, and carrier concentration provide insights into the mechanisms underlying the observed performance variations in the different charge cases.

It is evident that the following observations can be made: 1) devices with high charge

concentrations on the front-side exhibit a high electric-field intensity and a high carrier concentration ratio; 2) devices with no or weak charge cases show a low electric-field strength and a high carrier concentration ratio near the front-side, leading to a low *PCE*; 3) the electric field direction for the positive charge case is from the front-surface to the interior, while for the negative charge case, it is the opposite (as depicted in **Figure 3.13**c); 4) in the positive charge case, a similar n^+/n junction is induced near the front-surface, causing the majority/minority carriers near the front-surface to be electrons/holes, respectively; 5) in the negative charge case, the majority/minority carriers switch from holes/electrons to electrons/holes from the front-surface to the interior (as shown in **Figure 3.13**d). This implies that a p^+ inversion layer is induced by the negative charge; 6) comparatively, cases with $Q_f = -10^{13}$ cm^{-2} have a slightly higher electric field strength and carrier concentration ratio than cases with $Q_f = +10^{13}$ cm^{-2}. This slight difference in ΔV is also the reason why the *PCE* of $Q_f = -10^{13}$ cm^{-2} is higher than that of $Q_f = +10^{13}$ cm^{-2}; 7) the electric field strength for $Q_f = -10^{11}$ cm^{-2} is slightly higher than that of the case with $Q_f = +10^{11}$ cm^{-2}. In this study, an *n*-type substrate is used, and when the interface charge is positive, the induced electrons accumulate on the surface of c-Si. This causes the Fermi level at the interface to be pulled close to the conduction band, resulting in a high ratio of majority/minority carriers and high efficiency. On the other hand, when the interface charge is negative (with a small amount of charge), the induced hole accumulates on the surface of the c-Si. As a result, the Fermi energy level at the interface is pulled close to the center of the band gap, leading to a high ratio of majority/minority carriers and a low efficiency. Consequently, the efficiency is reduced in this case. However, when the negative charge at the interface is large, the induced hole accumulates on the surface of the c-Si, causing the Fermi energy level at the interface to be pulled close to the valence band. This results in a high ratio of majority/minority carriers and high efficiency, similar to the positive charge case. The energy level position at the interface undergoes significant changes compared to the c-Si substrate, leading to a higher electric field and a higher ratio of majority/minority carriers at the interface. In summary, for *n*-type silicon, positive charges are generally a better choice as they result in higher efficiency. However, in

extreme cases with a large amount of charge, negative charges can also achieve high efficiency.

Furthermore, **Figure 3.14**a displays the carrier concentration distributions to address the valley *PCE* observed for $Q_f = -3\times10^{10}$ cm^{-2}. Compared to the case with no charge, the presence of weak charge leads to a high concentration of minority carriers in the front-side of the Si. This, in turn, increases carrier recombination loss at the interface and results in a low *PCE*.

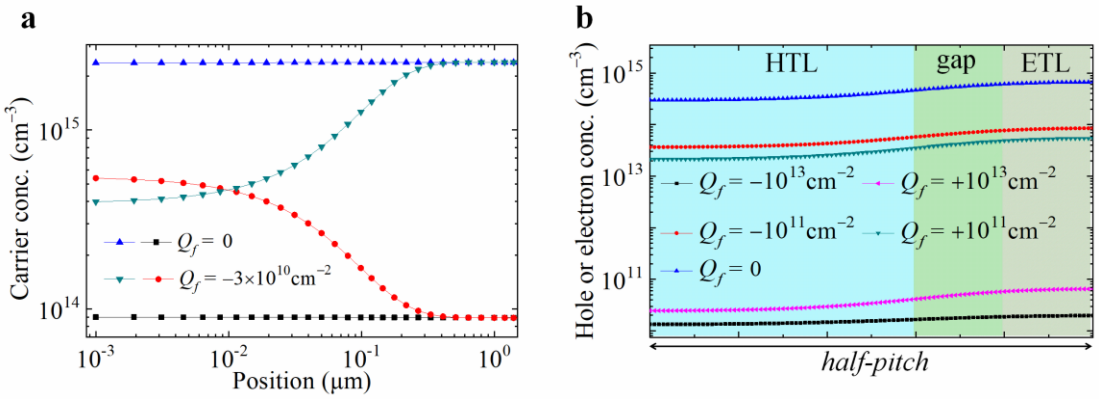

Figure 3.14 (a) Carrier concentration distributions along the vertical direction for cases of $Q_f = 0$ and -3×10^{10} cm^{-2}. (b) Concentration distributions of holes or electrons in the front-side of Si along the horizontal direction with different Q_f. Hole distributions are plotted for cases of $Q_f = 0$, $+10^{11}$ cm^{-2} and $+10^{13}$ cm^{-2}, while electron distributions for cases of $Q_f = -10^{11}$ cm^{-2} and -10^{13} cm^{-2}.

To provide a comprehensive understanding of the impact of interface charge on spatial parameter distributions, the corresponding results under light conditions are also presented in **Figure 3.15**. By comparing these plots, it can be observed that the two conditions exhibit similar trends. However, the advantages observed in the dark case, such as a high difference between the charge and no charge cases for potential, electric field, and carrier concentration ratio for the front-surface charge case, are diminished with the introduction of a large number of injected carriers under AM1.5G illumination.

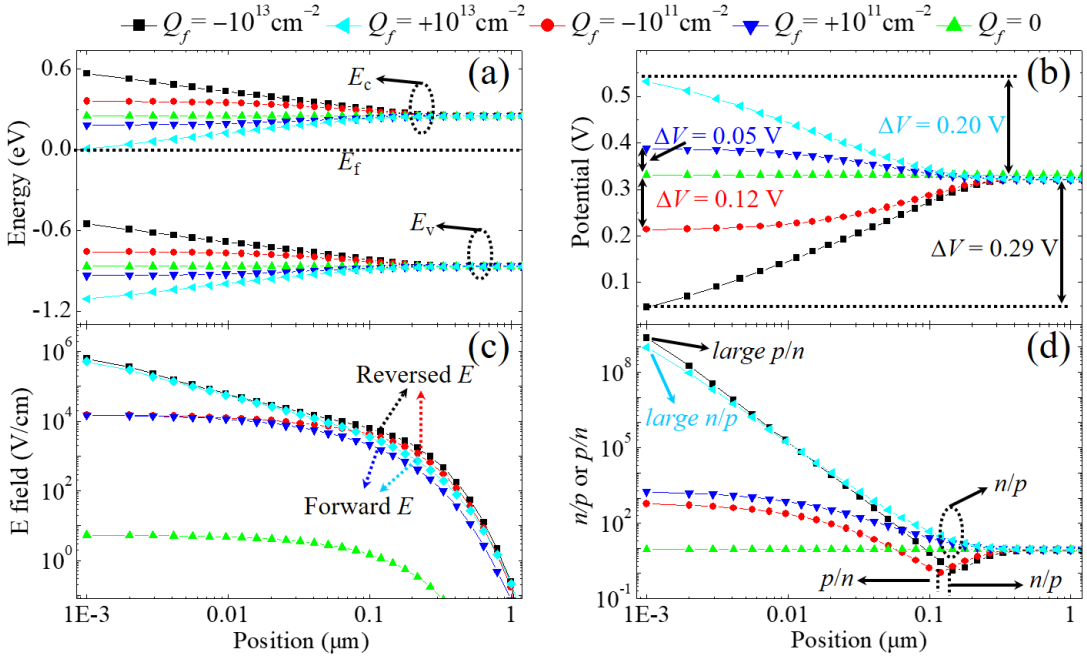

Figure 3.15 Position-dependent distributions of (a) energy, (b) potential, (c) internal electrical-fields and (d) charge-carrier concentration proportions under AM1.5 illustration.

Moreover, **Figure 3.14**b shows the concentration distributions of minority carriers at the front-side of the Si along the horizontal direction for different Q_f values. It reveals the following: 1) larger Q_f values dramatically suppress the concentration of minority carriers, leading to reduced recombination; 2) The regions above the ETL and the bandgap suffer from a higher concentration of minority carriers compared to the HTL. This indicates that the front-surface recombination, mainly caused by the above ETL and gap regions, exhibits an asymmetrical distribution along the horizontal direction.[124,136]

The front-surface Q_f has an impact on the carrier transport behavior of Si substrates and the interfaces of HTL/*n*-Si, gap/*n*-Si, and ETL/*n*-Si simultaneously. **Figure 3.16** presents the related results, where a low D_{it} of 10^{10} eV^{-1}cm^{-2} for the front DPTF/*n*-Si interface is fixed to eliminate the influence of recombination loss at the front surface. In **Figure 3.16**a, the *PCE* values are shown for different work functions of the HTL (WF_{HTL}) and the S_{HTL} under Q_f = 0. It reveals that the *PCE* depends on the S_{HTL} for cases where WF_{HTL} < 5.1 eV, while it is insensitive to the S_{HTL} for cases where WF_{HTL} >

5.1 eV. **Figure 3.16**b considers the three related interfaces (HTL/*n*-Si, gap/*n*-Si, and ETL/*n*-Si) with identical recombination velocities (*i.e.*, $S_{HTL} = S_{ETL} = S_{gap}$). It suggests that a significant decrement in *PCE* is observed when the interfaces are poorly passivated, and negative charge has a slight promoting effect on device performance.

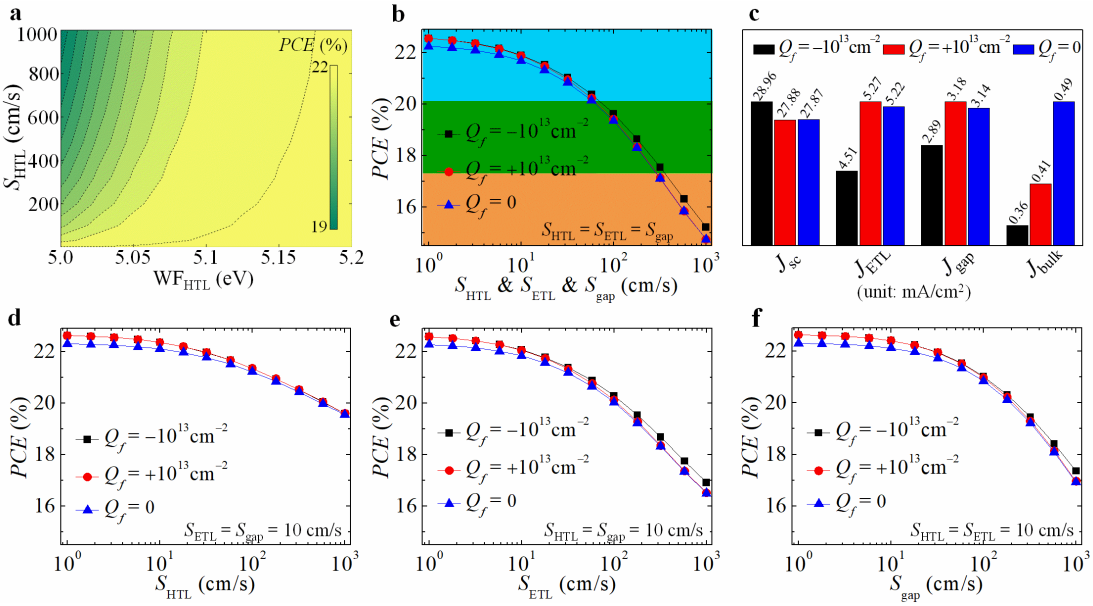

Figure 3.16 (a) *PCE* values as functions of S_{HTL} and WF_{HTL} for cases of $Q_f = 0$. (b) *PCE* values at the different S_{HTL}&S_{ETL}&S_{gap} for $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. Here, S_{HTL}, S_{ETL} and S_{gap} was fixed at 10 cm/s and S_{HTL}&S_{ETL}&S_{gap} means the same recombination velocity for the three interfaces. (c) J_{sc}, J_{ETL}, J_{gap} and J_{bulk} distributions for the three example Q_f. (d)/(e)/(f) *PCE* values under the different S_{HTL}/S_{ETL}/S_{gap} for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. Here, the charges are placed on the front surface of c-Si.

In **Figure 3.16**c, the corresponding distributions of J_{sc} and the current loss from the ETL/*n*-Si interface (J_{ETL}), gap/*n*-Si interface (J_{gap}), and bulk-Si (J_{bulk}) for the three samples under a surface recombination velocity (S_{eff}) of 1000 cm/s are listed. It reveals that the sample with negative charges exhibits a high J_{sc} value of 28.96 mA/cm^2, primarily due to lower recombination at the ETL/*n*-Si and gap/*n*-Si interfaces and Si substrates, with corresponding values of 4.51, 2.89, and 0.36 mA/cm^2, respectively. The positive charge case shows a slightly higher J_{ETL} value of 5.27 mA/cm^2 and J_{gap} value of 3.18 mA/cm^2 but a lower J_{bulk} value of 0.41 mA/cm^2 compared to the case with no

charge. This results in a degraded J_{sc} value of 28.88 mA/cm^2 for the positive charge case compared to the cases with negative charges. These results demonstrate that the positive charge case exhibits a slightly higher *PCE* when the interfaces are well-passivated, but almost the same *PCE* as the case with no charge when the interfaces are poorly passivated. When the carrier recombination velocity of the three related interfaces is less than 10 cm/s, the interface recombination loss is effectively suppressed, and Si bulk loss becomes the main recombination source, leading to a slightly higher *PCE* for the positive charge case. However, when the carrier recombination velocity of the three interfaces reaches 1000 cm/s, the main contributions to the recombination loss for the positive charge case come from the related interfaces, resulting in almost the same *PCE* as the case with no charge.

In **Figure 3.16**d, the three related samples with $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0 were further examined to investigate the relationship between front-surface charges and the HTL/*n*-Si interface, while keeping WF_{HTL} constant at 5.0 eV. It is evident from **Figure 3.16**d that: 1) when the HTL/*n*-Si interface is well-passivated (S_{HTL} < 10 cm/s), the *PCE* for all three cases remains relatively high; 2) with an increase in S_{HTL} from 10 to 1000 cm/s, the *PCE* values of the three related cases decrease sharply; 3) the *PCE* values of the positive charge case exhibit almost the same trend and values as the negative charge case. The ETL/*n*-Si and gap/*n*-Si interfaces are also shown in **Figure 3.16**e and **3.16**f, respectively, which display a similar trend to the HTL/*n*-Si case but with a larger reduction in *PCE*. However, unlike the HTL/*n*-Si case, in the positive charge case, when the passivation is good (S_{ETL} or S_{gap} < 10 cm/s), a slightly higher *PCE* is observed compared to the case with no charge. However, this effect is not observed when the passivation is poor enough (S_{ETL} or S_{gap} = 10 cm/s).

3.3.3 Passivation Mechanism

To further elucidate the mechanism by which front-surface charges improve *PCE*, the

electric-field distributions of the bulk-Si were examined in **Figure 3.17**. Taking a representative wavelength (600 nm) as an example, the spatial electric-field distributions were analyzed. Upon careful observation, it becomes evident that the electric-field strength within the Si substrates, except near or above the gap region, is enhanced in the front-surface charge cases compared to the case with no front-surface charge, as shown in **Figure 3.17**a-**3.17**c. This strengthening of the electric field contributes to a lower J_{bulk} (bulk current density).

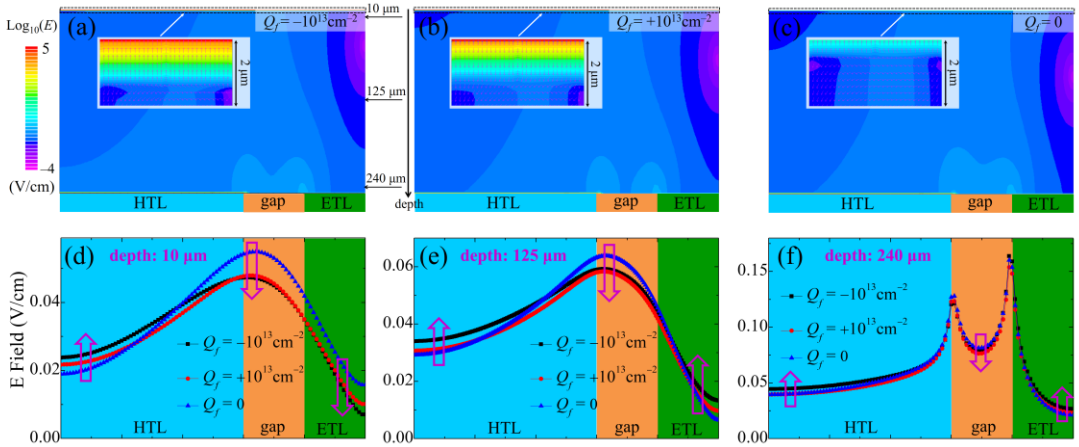

Figure 3.17 (a)-(c) Electric-field distributions for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0 under AM1.5G with a typical wavelength of 600 nm, respectively. (d)-(f) Cross-sectional electric-field distributions in the horizontal direction within the *half-pitch* under the depths of 10 μm, 125 μm and 240 μm.

Specifically, the electric-field distributions along the horizontal direction at depths of 10, 125, and 240 μm are plotted in **Figure 3.17**d-**3.17**f. These plots reveal that the electric-field intensity is strengthened within the HTL and ETL regions in cases with charges on the front side, up to depths of 125 and 240 μm. However, above the gap region, the electric-field intensity is weakened. This indicates that front-surface charges assist in extracting carriers to the relevant transport regions, widening the carrier transport channel, improving carrier selectivity, and reducing recombination losses.

The impact of front-surface charges on device performance under various Si substrate

thicknesses is illustrated in **Figure 3.18**. The Δ*PCE*, defined as the *PCE* difference between the front-surface charge case and the no charge case, is presented. It is evident from **Figure 3.18**a that Δ*PCE* increases rapidly for the negative charge case as the Si thickness decreases from 500 to 50 μm. This suggests that the performance of devices with thinner Si substrates is more susceptible to negative charge effects. In contrast, the positive charge case exhibits minimal impact on cell performance, with Δ*PCE* remaining close to zero. This conclusion is further supported by the average internal quantum efficiency (*IQE*) shown in **Figure 3.18**b. As the Si thickness decreases from 500 μm to 50 μm, *IQE* decreases on average from 0.91 to 0.77 for the negative charge case, while it increases from 0.7 to 0.75 for the positive/no charge cases. In order to better understand the significant increase in *PCE* for the negative charge case with a thinner Si substrate, the distributions of hole concentrations at a depth of 25 μm and the corresponding current density (J_h) across the entire Si region were presented in **Figure 3.18**c and **3.18**e-**3.18**f, respectively. These results were obtained using a thinner system with a 50 μm-thick Si substrate and a reference wavelength of 600 nm. **Figure 3.18**c shows that the hole concentration in the HTL region is improved for the negative charge case, while it is reduced in the ETL and gap regions. This variation in hole concentration is responsible for the lower recombination, higher *IQE*, and higher *PCE* observed in **Figure 3.18**a-**3.18**b. The J_h distributions in **Figure 3.18**d-**3.18**f clearly demonstrate that the J_h above the gap and ETL regions is weakened for the negative charge case compared to the positive and no charge cases, as depicted in **Figure 3.18**d-**3.18**f. This reduction in current density leads to a decreased recombination loss. For a more intuitive comparison, the J_h distributions along the horizontal direction at a depth of 25 μm are shown in **Figure 3.18**e-**3.18**f.

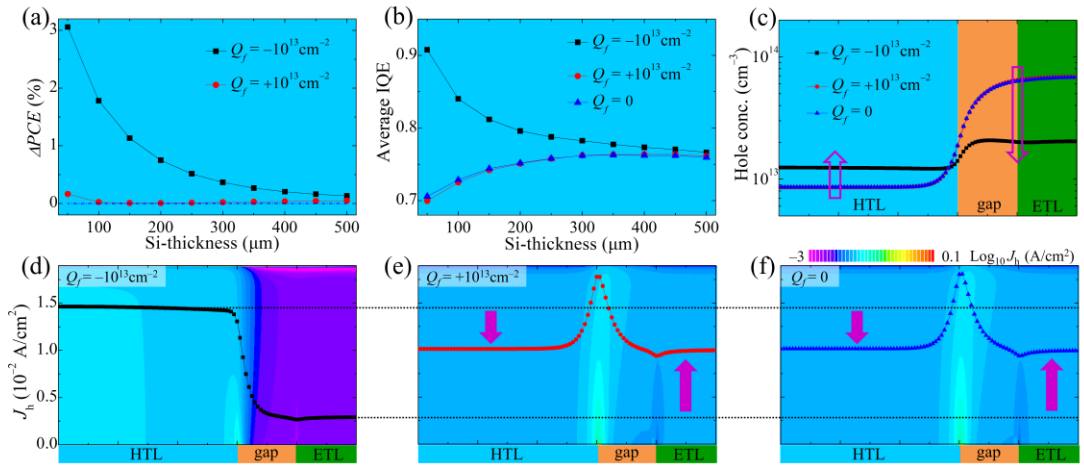

Figure 3.18 (a) ΔPCE under the different Si thicknesses for the two related cases. (b) The average IQE values under the different Si thicknesses for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. (c) Concentration distributions of holes with the Si thickness of 50 μm along the horizontal direction at a depth of 25 μm for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. The carriers recombination ratios of S_{HTL}, S_{ETL} and S_{gap} were kept at 1000 cm/s. (d)-(f) Cross-sectional distributions of J_h in the whole bulk-Si under a 50 μm-thick Si substrate for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively.

Furthermore, the corresponding J_h distributions under a 500 μm-thick Si substrate in **Figure 3.19** exhibit similar values for all three cases, indicating that the front-surface charge is not effective for thicker Si substrates.

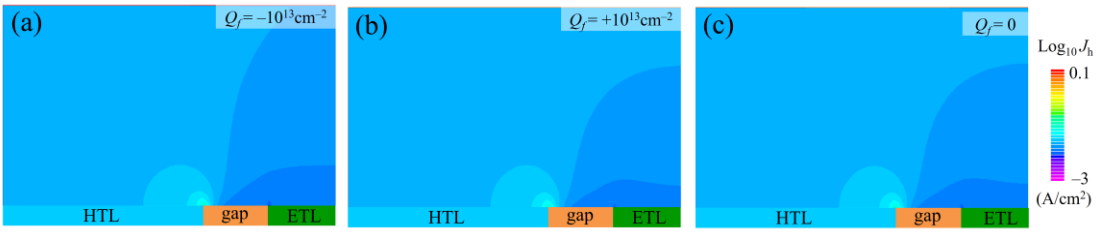

Figure 3.19 (a)-(c) J_h distributions inside the 500 μm thick bulk-Si for the cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively.

3.3.4 Conclusion

An approach has been proposed to enhance the front-surface passivation in IBC-HJ solar cells by utilizing the interface charge inherent in the dielectric passivation thin

films. The impact of this approach on the *PCEs* of IBC devices, as well as the front-surface Q_f and D_{it}, was investigated theoretically. The results demonstrate the following: 1) a high *PCE* can be achieved when the front-surface charge density exceeds 5×10^{12} cm^{-2} or when the front-surface is well-passivated with a low D_{it} value of less than 10^{10} $eV^{-1}cm^{-2}$; 2) the presence of a large front-surface Q_f exhibits high tolerance to D_{it}; 3) in cases where $Q_f > 10^{12}$ cm^{-2}, the negative charge exhibits a slightly higher *PCE* compared to the positive charge case due to the higher potential and stronger electric field. The energy band, potential, electric field, and carrier concentration ratio near the front-surface were analyzed to explain the increase in *PCE*. It was found that the front-surface charge also has a positive impact on the bulk-Si region, promoting carrier transport throughout the entire Si region and partially suppressing recombination losses at the interfaces of HTL/*n*-Si, ETL/*n*-Si, and gap/*n*-Si. This is attributed to the strengthened electric field within the entire relevant region. These results provide valuable design principles for incorporating front-surface charges, offering broad guidance for achieving high-efficiency IBC-HJ solar cells.

3.4 Gap Charge Passivation

3.4.1 Simulation Details

A 250 μm-thick *n*-type doped Si substrate with a doping concentration (N_d) of 2.3×10^{15} cm^{-3} was utilized in the study. A dopant-free system with a double planar structure was

employed, consisting of a 5 nm-thick thin a-Si:H(*i*) layer and a Si_3N_4 film with a thickness of 75 nm, serving as the front-sided antireflection coating (ARC) and/or passivation layer. The work function of the HTL was kept constant at 5.3 eV.[137] The energy band alignment at the electron transport layer (ETL)/*n*-Si contact was assumed to be flat. The wavelength range of 300 to 1200 nm was considered for the simulations of the IBC-HJ solar cells using Silvaco TCAD software.[138] The electrical parameters such as mobility, lifetime, and recombination coefficients were obtained from relevant references[27,31,130], which were also list in Table 3.3.

Table 3.3 Electrical parameters for this simulation.

Parameters	Values
Donor doping concentration (N_d) of Si substrate	2.3×10^{15} cm^{-3}
Thickness of Si substate	250 μm
Lifetime of Si substrate	3 ms
Electron/hole mobility of Si substrate	1000/800 cm^2/Vs
$f_{HTL}/f_{gap}/f_{ETL}$	0.6/0.2/0.2
Pitch	2000 μm
a-Si:H(*i*)/Al_2O_3 ARC	7/75 nm
Recombination ratio of HTL/*n*-Si	10 cm/s
Recombination ratio of gap/*n*-Si	10 cm/s
Recombination ratio of ETL/*n*-Si	10 cm/s
Work function of HTL	5.3 eV

Figure 3.20a, **3.20**c, and **3.20**e illustrate the simulated configurations of the IBC solar cells for cases with no, negative, and positive built-in charges at the rear gap/*n*-Si interface, respectively. In the absence of fixed charges, the energy band near the rear gap surface remains nearly flat, resulting in a large number of minority carriers near the rear gap/*n*-Si interface and, consequently, strong carrier recombination losses (**Figure 3.20**b).

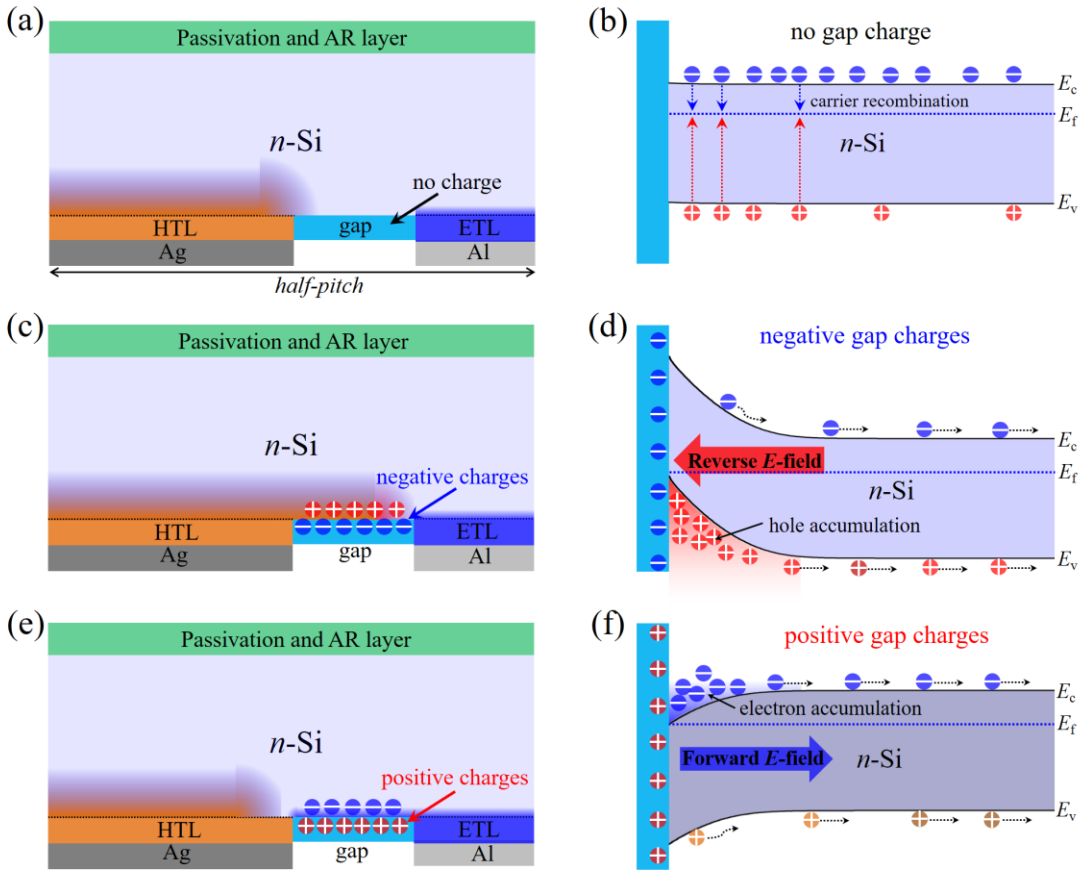

Figure 3.20 Sketch maps/the corresponding energy band diagram near rear gap surface of Si-based IBC devices for cases of (a)/(b) none, (c)/(d) negative and (e)/(f) positive charges at rear gap/*n*-Si interface.

By introducing negative or positive fixed charges at the rear gap/*n*-Si interface (**Figure 3.20**d/**3.20**f), holes or electrons are attracted towards the fixed charges and accumulate at the rear gap surface. This accumulation of carriers causes an energy band offset, where the energy band edges of negative or positive fixed charges are close or far from the vacuum energy reference, respectively. When the Q_f value is sufficiently large, a strong reverse or forward electric field induced by the negative or positive fixed charges (**Figure 3.20**d/**3.20**f) impedes the transport of electrons or holes into the rear gap surface. As holes or electrons continuously accumulate in the valence or conduction band, they reach a saturation state under thermal equilibrium, and the accumulated carriers are pushed away from the rear gap surface due to the electrostatic field created by the accumulated carriers. Consequently, carrier recombination at the rear gap surface

can be effectively suppressed due to the energy band offset caused by the fixed charges and the beneficial electrostatic field, which applies to both negative and positive fixed charges.

3.4.2 Passivation Effect

Since surface recombination was dominated by the interface defect and the minority carrier concentration,[135] the relationship between the *PCE* and the rear-gap surface recombination ratio (S_{gap}) and the fixed charge density (Q_f) inherent to the dielectric passivation film at the rear gap region was investigated, as shown in **Figure 3.21**a. The surface recombination ratios at the interfaces of the rear-sided hole transport layer/*n*-Si (S_{HTL}), electron transport layer/*n*-Si (S_{ETL}), and front-side passivation layer/*n*-Si (S_{front}) were all kept constant at 10 cm/s. The *pitch* of the devices was maintained at a constant of 2000 μm, with area fill proportions of 0.6, 0.2, and 0.2 for HTL (f_{HTL}), gap (f_{gap}) and ETL (f_{ETL}), respectively.

From **Figure 3.21**a, the following observations can be made: 1) a remarkable *PCE* over 20% can be expected if $|Q_f|$ is larger than 10^{12} cm^{-2}; 2) for a lower Q_f value, less than 10^{11} cm^{-2}, a high-quality passivation with a S_{gap} less than 10 cm/s can result in an outstanding *PCE*; 3) the minimal *PCE* is located at $Q_f \sim -3\times10^{10}$ cm^{-2}, as indicated by the white arrow. For comparison, the *PCE* ratios, PCE_{+Qf}/PCE_{-Qf}, were plotted in **Figure 3.21**b. The plot reveals that cases with positive fixed charges show a higher *PCE* than cases with negative fixed charges if $|Q_f|$ is less than 2×10^{11} cm^{-2}. However, cases with negative fixed charges achieve a higher *PCE* value than positive fixed charges when $|Q_f|$ exceeds 5×10^{11} cm^{-2}. To assess the impact of the gap size (f_{gap}) and the doping concentration (N_d) of the silicon substrate on device performance, the variation of *PCE* of this kind of IBC solar cells under different f_{gap}/N_d and Q_f values was shown in **Figure 3.21**c/**3.21**d, with S_{gap} kept constant at 10^3 cm/s. A poor gap passivation with $S_{gap} = 10^3$ cm/s was considered to maximize the impact of the related

parameters on cell performance. **Figure 3.21**c exhibits a similar dispersion relationship to **Figure 3.21**a. It suggests that reducing S_{gap} can effectively improve the *PCE* of IBC-HJ solar cells if Q_f is not sufficiently high (< 10^{11} cm^{-2}). However, even if f_{gap} is small enough (f_{gap} = 0.01), it cannot completely suppress carrier recombination losses.

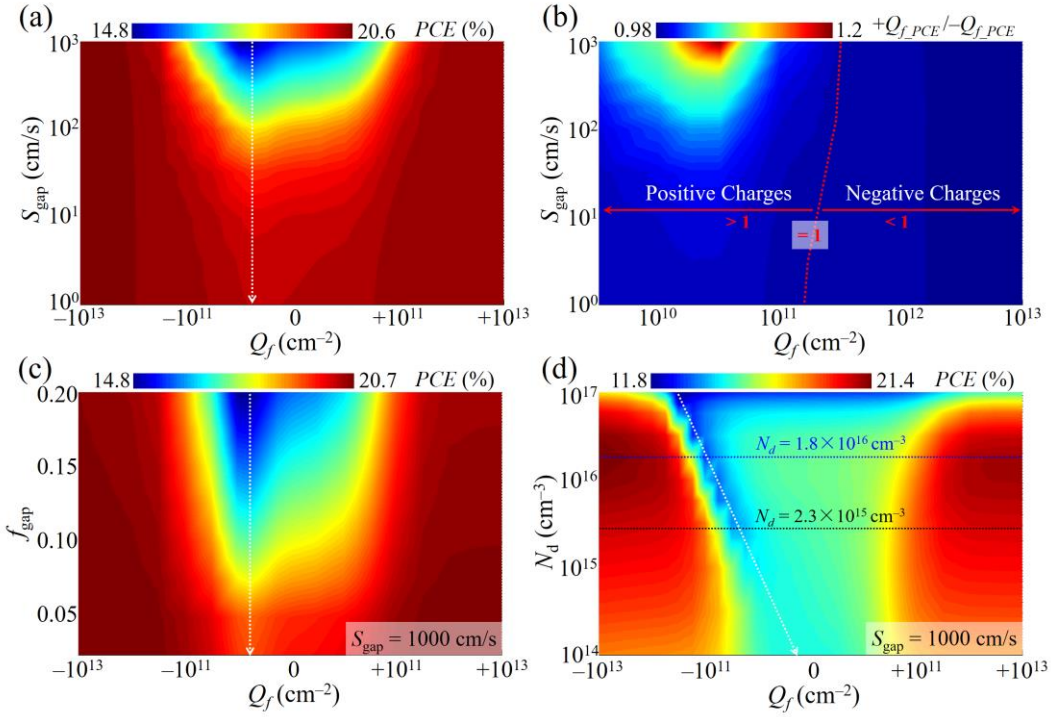

Figure 3.21 (a) *PCE* values of IBC SCs as functions of S_{gap} and Q_f. (b) *PCE* ratios versus D_{it} and Q_f. (c) *PCE* values versus f_{gap} and Q_f under a fixed S_{gap} of 10^3 cm/s, in which f_{ETL} was kept at a constant of 0.2. (d) *PCE* values versus N_d and Q_f at a fixed S_{gap} of 10^3 cm/s and a fixed $f_{HTL}/f_{gap}/f_{ETL}$ of 0.6/0.2/0.2.

The relationship between N_d, Q_f, and *PCE* was plotted in **Figure 3.21**d, indicating that *PCEs* under S_{gap} = 10^3 cm/s exhibit an increasing trend followed by a decrease with the increase of N_d from 10^{14} to 10^{17} cm^{-3}, yielding an optimized N_d of 1.8×10^{16} cm^{-3}. This conclusion is consistent with the results in **Figure 3.8**. The non-monotonous relation between the N_d and the *PCE* observed in the results is influenced by multiple factors within the device structure. When the doping concentration is low (N_d < 1.8×10^{16} cm^{-3} in this case), the V_{oc} of the device is lower. When the doping concentration is high (N_d > 1.8×10^{16} cm^{-3}), the *FF* of the device rapidly decreases. Therefore, there exists an

optimized doping concentration (1.8×10^{16} cm^{-3} in this case) where the *PCE* is maximized. This optimized doping concentration balances the trade-off between the V_{oc} and the *FF*, resulting in the highest overall efficiency for the given device structure. Moreover, with the increase of N_d from 10^{14} to 10^{17} cm^{-3}, the minimal *PCE* values decrease, while the corresponding Q_f values increase, as shown by the white arrow.

The inherent charges present in the rear-side gap region, as discussed above, have a positive impact on the carrier transport channel and surface passivation at the rear gap/*n*-Si interface. However, the variations in the carrier transport process will also affect other related interfaces, such as the HTL/*n*-Si and ETL/*n*-Si interfaces. Therefore, the relationship between S_{ETL}, f_{ETL}, and cell size with device performance needs to be examined, as shown in **Figure 3.22**. S_{HTL} and f_{HTL} were not discussed because the high electric field intensity near the HTL surface (~10^6 V/cm) provides high-quality passivation, which remains largely unchanged even in the presence of fixed charges at the rear gap, resulting in minimal impact on the cell's *PCE* due to S_{HTL} and f_{HTL}. With an increase in S_{ETL} from 1 to 10^3 cm/s, the *PCEs* for all three cases decrease. However, the case with $Q_f = -10^{13}$ cm^{-2} can still maintain a relatively high *PCE* to some degree, as shown in **Figure 3.22**.

The *PCE* differences (ΔPCE) between the cases with positive or negative fixed charges and no fixed charges were also plotted in **Figure 3.22**. It is observed that the case with fixed negative charges under $S_{ETL} = 10^3$ cm/s has a favorable impact on *PCE*, with ΔPCE exceeding 1.2%, while the case with fixed positive charges is almost ineffective. The relevant electrical parameters under $S_{ETL} = 10^3$ cm/s are listed in the histogram shown in **Figure 3.22**b. The case with $Q_f = -10^{13}$ cm^{-2} shows a slightly lower V_{oc} and *FF* compared to the cases with $Q_f = +10^{13}$ cm^{-2} and 0. However, it exhibits a very high J_{sc}, which is 31.64/28.60/28.63 mA/cm^2 for the cases of $Q_f = -10^{13}/+10^{13}/0$ cm^{-2}. The significant improvement in J_{sc} by 3 mA/cm^2 for the case of $Q_f = -10^{13}$ cm^{-2} is due to reduced interface recombination at the ETL/*n*-Si interface, resulting in a higher *PCE* of 17.02%. **Figure 3.22**c and **3.22**d demonstrate the *PCE* and ΔPCE as a function of f_{ETL}

and *half-pitch*, respectively. Similar to the results in **Figure 3.22**a, increasing f_{ETL} and half-pitch for all three cases leads to a decrease in *PCE*. However, this degradation can be alleviated for cases with fixed negative charges at the rear gap/*n*-Si interface.

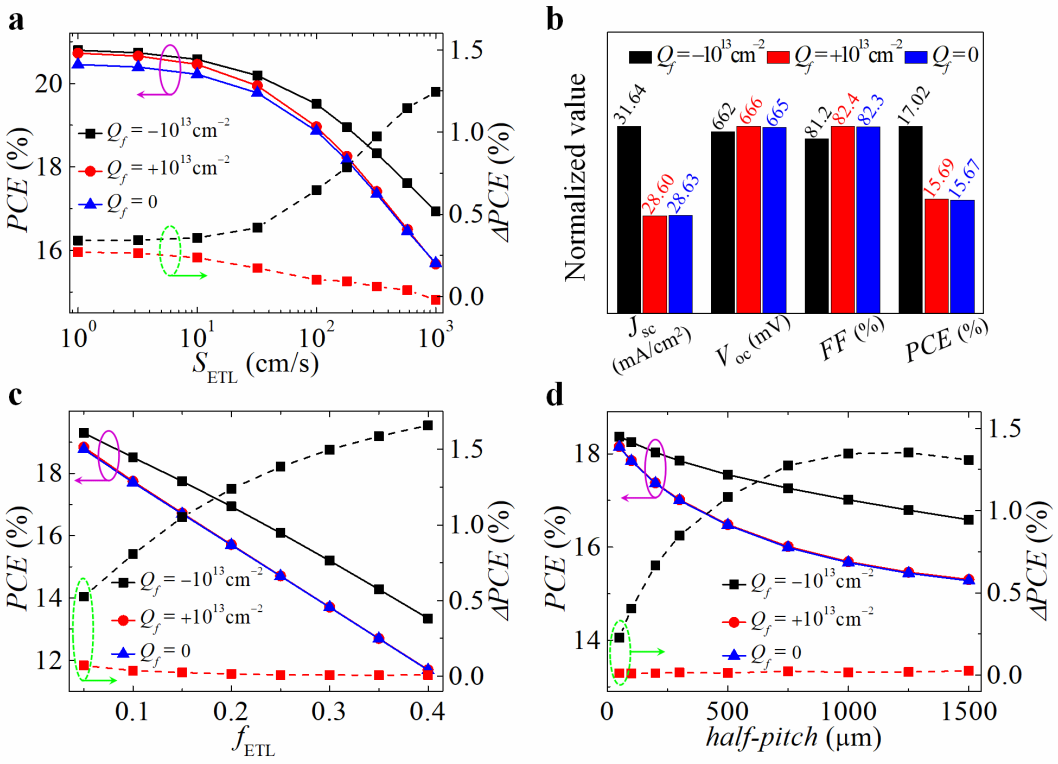

Figure 3.22 (a)/(c)/(d) *PCE* and Δ*PCE* (*i.e.*, the *PCE* differences between the cases with positive or negative fixed charges and no fixed charges) values versus S_{ETL}/f_{ETL}/*half-pitch* under the cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. (b) Electrical parameter distributions including J_{sc}, V_{oc}, *FF* and *PCE* for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0 under $S_{ETL} = 10^3$ cm/s.

Apart from the rear HTL, gap, and ETL, the fixed charges at the rear gap also impact the carrier transport process within the Si substrates and the front-side surface. The effect of front-side surface passivation quality on device performance was examined under three representative cases: $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2}, and 0, as shown in **Figure 3.23**a. The recombination velocities at the three rear interfaces were kept constant at 10 cm/s (*i.e.*, $S_{HTL} = S_{gap} = S_{ETL} = 10$ cm/s). It is observed that as S_{front} increases from 1 to 100 cm/s, there is a significant reduction in *PCE* for all three cases. However, the case with $Q_f = -10^{13}$ cm^{-2} shows the smallest decrease, indicating that fixed negative charges

at the rear gap region have a positive effect on the front-side surface passivation. For cases with low passivation levels of the front-side surface (S_{front} = 100 cm/s), the largest *PCE* difference (Δ*PCE*) between negative fixed charges and no charges can be up to 1%.

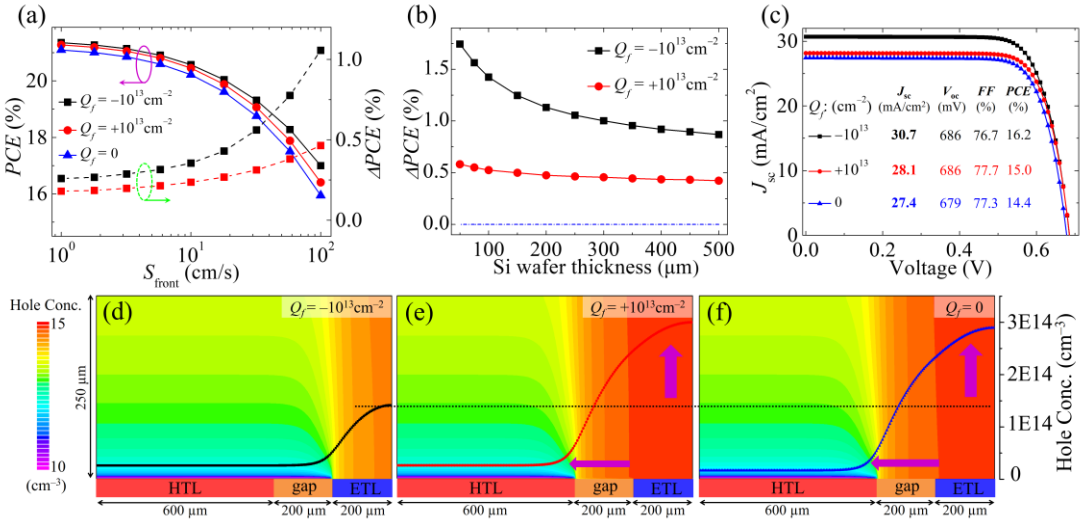

Figure 3.23 (a) *PCE* and Δ*PCE* values under the different S_{front} for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0. (b) Δ*PCE* values under the different thicknesses of Si substrates for cases of $Q_f = -10^{13}$ cm^{-2} and $+10^{13}$ cm^{-2}. (c) Light *J-V* curves for the three related samples under a 50 μm-thick Si substrate. The inset lists the photoelectrical parameters extracted from the related plots. (d)-(f) Hole concentration distributions within *half-pitch* under a 50 μm-thick Si substrate for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively. Recombination velocities of three related rear interfaces were kept as a constant at 10 cm/s, *i.e.*, $S_{HTL} = S_{gap} = S_{ETL}$ = 10 cm/s.

The relationship between cell performance and Si wafer thickness was investigated as shown in **Figure 3.23**b, considering poor front surface passivation with S_{front} = 100 cm/s. The Δ*PCEs* for both positive and negative fixed charges exhibit a sharp decrease followed by a plateau as the Si substrate thickness increases from 50 to 500 μm (the case with negative fixed charges has higher Δ*PCE* values than the case with positive fixed charges). This indicates that front surface passivation with a thinner Si wafer is more susceptible to the charges inherent to the rear-side gap region. For a direct comparison, the *J-V* characteristic curves, along with the relevant electrical parameters,

for the cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2}, and 0 under a 50 μm-thick Si substrate, are shown in **Figure 3.23**c. Clearly, the increased *PCEs* for cases with fixed charges stem from the enhanced J_{sc}.

In this dopant-free system, minority carriers drive the transport/recombination/collection process. Thus, the hole concentration in the *n*-Si wafer is crucial to confirm the strengthened front-surface passivation by the rear gap charges. **Figure 3.23**d-**3.23**f illustrate the hole concentration distributions within a 50 μm-thick Si substrate for the cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2}, and 0, respectively. For the case of -10^{13} cm^{-2}, a very low hole concentration within the bulk Si (especially near the gap and ETL regions) can be observed compared to the other two cases. Specifically, the cut-line hole concentrations at the front Si surface for the three cases are plotted in the figure. It is evident that the hole concentration near the gap and ETL regions for the case of $Q_f = -10^{13}$ cm^{-2} is approximately half as high as that for the case of $Q_f = +10^{13}$ cm^{-2} and 0. This reveals low front surface recombination and a high J_{sc} for the case of $Q_f = -10^{13}$ cm^{-2}, as shown in **Figure 3.23**c.

Furthermore, the hole concentrations at the front Si surface under different Si substrate thicknesses were demonstrated in **Figure 3.24**. It is observed that with the increase in Si thickness from 50 to 250 μm and 500 μm, the hole concentrations for all three cases ($Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2}, and 0) increase. However, the differences in hole concentration between the case of $Q_f = -10^{13}$ cm^{-2} and the cases of $Q_f = +10^{13}$ cm^{-2} and 0 are enlarged, particularly for the regions near the gap and ETL. This indicates that for a low-level passivation of the front surface, the thin Si wafer strongly relies on the fixed charges at the rear gap, especially the negative charges. In contrast, the thick Si wafer is almost independent of the fixed charges at the rear gap.

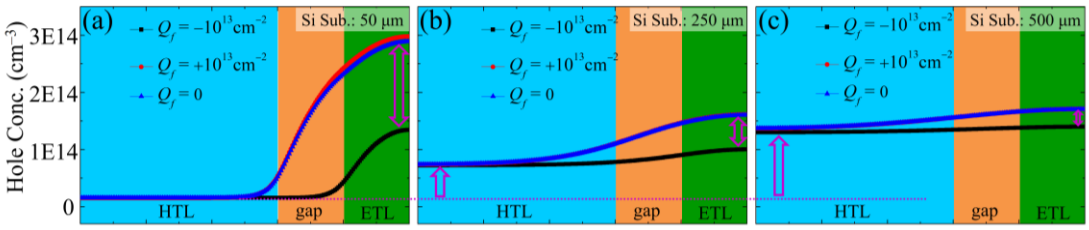

Figure 3.24 (a)-(c) Cross-sectional distributions of hole concentrations for the different thickness of Si substrates with rear gap Q_f of -10^{13} cm^{-2}, $+10^{13}$ cm^{-2} and 0. These plots are cut-line hole concentration distributions at the front passivation layer/c-Si interface.

3.4.3 Passivation Mechanism

To better understand the passivation mechanism of the fixed charges inherent to the rear-side gap region, carrier concentrations and energy bands are illustrated in **Figure 3.25**a-**3.25**c. Different cases are considered with varying values of Q_f, including $\pm10^{13}$ cm^{-2}, $\pm10^{11}$ cm^{-2}, and 0. In the case of $Q_f = 0$, the energy band is nearly flat under thermal equilibrium, resulting in a constant distribution of hole and electron concentrations, as shown in **Figure 3.25**a and **3.25**b. For cases with fixed positive charges at the rear-side gap surface, a downward energy band offset is formed, leading to a decrease in hole concentration and an increase in electron concentration near the rear gap region, as depicted in **Figure 3.25**a and **3.25**b. On the other hand, for cases with negative fixed charges, an upward energy band offset is formed, resulting in the formation of a *p*-type inversion layer near the rear gap surface. This inversion layer prevents electrons from transporting into the rear gap surface, leading to a decrease in electron concentration, as illustrated in **Figure 3.25**a and **3.25**b. Clearly, both positive and negative fixed charges induce energy band offsets, reduce carrier concentrations at the surface, and suppress carrier recombination near the rear gap surface.

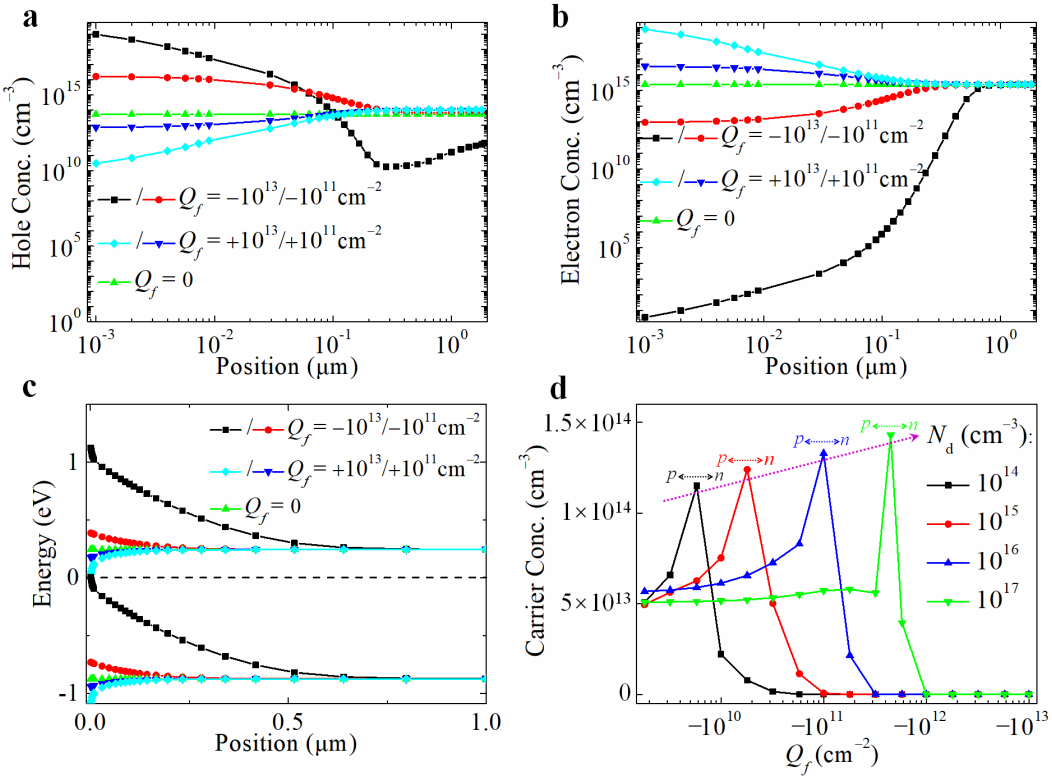

Figure 3.25 Position-dependent (a)/(b) concentrations of holes/electrons and (c) energy levels for cases of Q_f = 0, ±10^{11} and ±10^{13} cm^{-2}. (d) Minority carrier concentrations at rear gap surface under the different Q_f.

In more detail, when comparing the case of Q_f = 10^{13} cm^{-2} with Q_f = 10^{11} cm^{-2}, it is observed that Q_f = 10^{11} cm^{-2} is not sufficient to induce a significant energy band offset, resulting in a lower *PCE*. To further explain the conclusions under various N_d values, the minority carrier concentrations at the rear gap surface are plotted in **Figure 3.25**d. Here, it is worth noting that negative charge attracts positive holes to the surface, leading to an increased hole concentration. However, if negative charge is high enough, the hole concentration is higher than that of the electron concentration. In this case, the minority carrier is electrons not holes. For the four relevant cases, the minority carrier concentrations initially increase and then decrease as Q_f increases from –10^{9} cm^{-2} to –10^{13} cm^{-2}. Here, minority carriers refer to holes/electrons to the left/right of the peak. Clearly, with increasing N_d from 10^{14} to 10^{17} cm^{-3}, the peaks of minority carrier concentrations show an increasing trend and shift to the right. It is reasonable to understand that higher N_d values require larger Q_f to shift the Si Fermi level closer to

the middle of the bandgap, thus causing the peak of minority carrier concentration to shift towards higher Q_f values.

Furthermore, electric field distributions were investigated to elucidate the carrier transport mechanism, as depicted in **Figure 3.26**. Three representative cases with Q_f values of -10^{13} cm^{-2}, $+10^{13}$ cm^{-2}, and 0 were taken as examples. It can be observed from **Figure 3.26**a-**3.26**c that the electric field for these cases exhibits similar distributions except in the rear-side gap region. Specifically, cut-line electric field profiles within the half-pitch at depths of 0.001, 1, and 10 μm were plotted in **Figure 3.26**d-**3.26**f, respectively. At the rear gap surface (at a depth of 0.001 μm), as shown in **Figure 3.26**d, the electric field intensity for the cases of $Q_f = \pm 10^{13}$ cm^{-2} is approximately 7 orders of magnitude higher than that for the case without fixed charges. This significant increase in electric field intensity is the main reason for the improved PCE in cases with fixed charges.

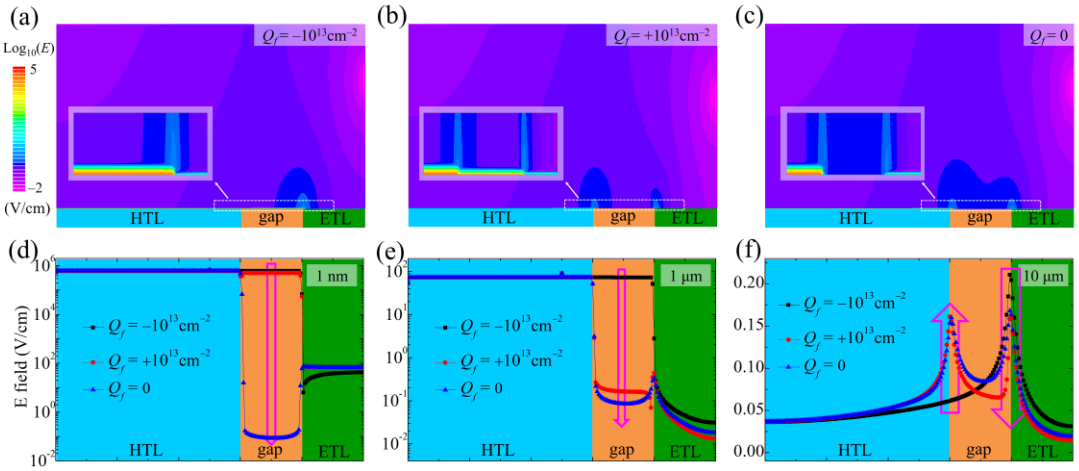

Figure 3.26 (a)-(c) Electric-field distributions for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively, under AM1.5G illumination at the wavelength of 600 nm with $S_{gap} = 10^3$ cm/s. (d)-(f) The cut-line electric-field distributions within *half-pitch* under three depths of 0.001 μm, 1 μm and 10 μm.

At a depth of 1 μm, as depicted in **Figure 3.26**e, a strong electric field is observed for the case of $Q_f = -10^{13}$ cm^{-2}, while a weaker electric field is observed in the gap region

for the cases of $Q_f = +10^{13}$ cm^{-2} and 0. When the depth increases to 10 μm, as shown in **Figure 3.26**f, a weak electric field is observed for all three cases, with one peak at the HTL/gap interface for the case of $Q_f = -10^{13}$ cm^{-2}, and two peaks at the HTL/gap and gap/ETL interfaces for the cases of $Q_f = +10^{13}$ cm^{-2} and 0.

To gain further insight into the carrier transport mechanism, the distributions of hole current density (J_{hole}) and electron current density ($J_{electron}$) were displayed in **Figures 3.27** and **3.28**, respectively. For $Q_f = -10^{13}$ cm^{-2}, a hotspot with high J_{hole} was observed at and near the gap/ETL interface. This hotspot was transferred to the HTL/gap interface for $Q_f = +10^{13}$ cm^{-2} and 0. The cut-line J_{hole} profiles shown in **Figure 3.27**d indicate high/medium/low J_{hole} values at the rear gap interface (at a depth of 0.001 μm) for $Q_f = -10^{13}/0/+10^{13}$ cm^{-2}, indicating that holes for the case of negative fixed charges transport along the rear gap interface.

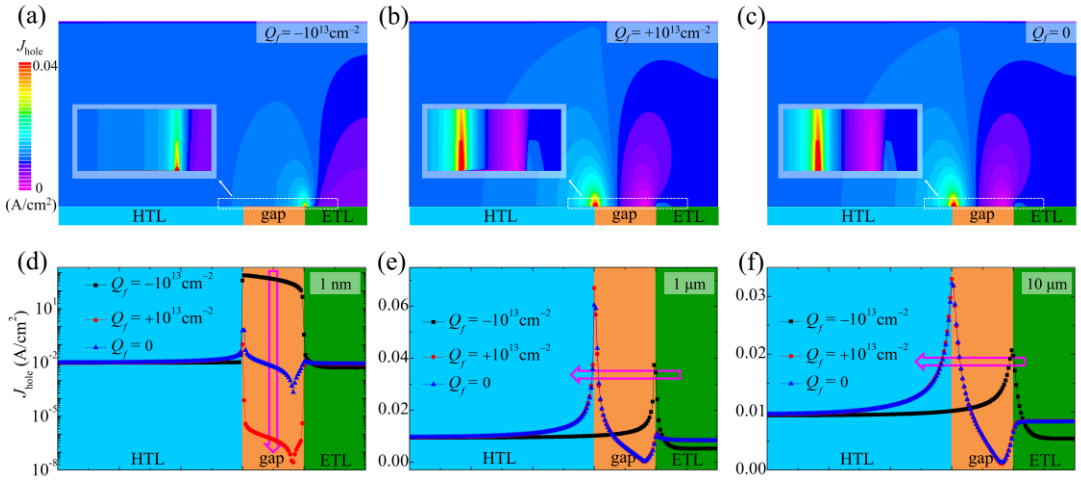

Figure 3.27 (a)-(c) Distributions of hole current density (J_{hole}) for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively. (d)-(f) Cut-line J_{hole} under the depths of 0.001, 1 and 10 μm, respectively.

The transferred peaks in **Figure 3.27**e and **3.27**f show that holes inside the bulk Si concentrate at the gap/ETL interface (for the case of $Q_f = -10^{13}$ cm^{-2}) and the gap/HTL interface (for the cases of $Q_f = +10^{13}$ cm^{-2} and 0). On the other hand, $J_{electron}$ distributions in **Figure 3.28** demonstrate that hotspots for all three cases are located at the same positions, indicating that the electron transport channel inside the bulk Si is almost

independent of the rear gap fixed charges.

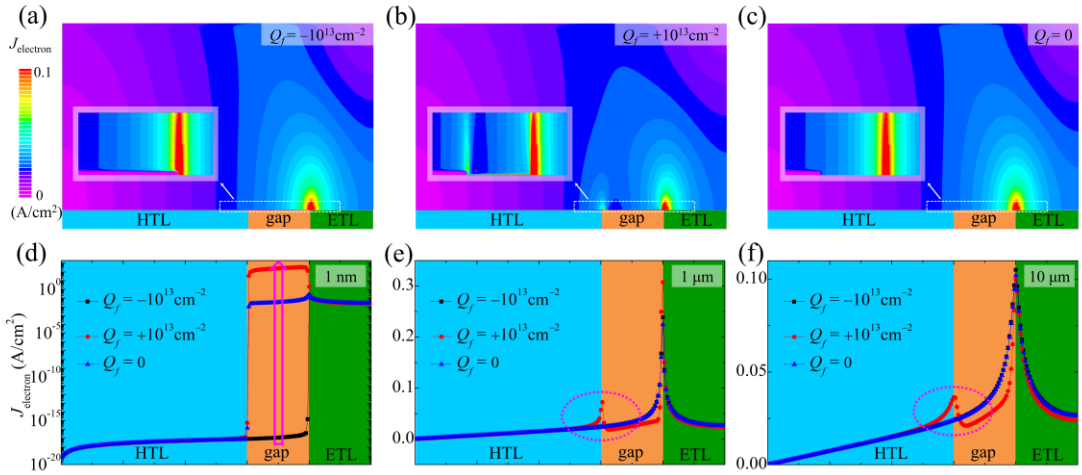

Figure 3.28 (a)-(c) Distributions of electron current density ($J_{electron}$) for cases of $Q_f = -10^{13}$ cm^{-2}, $+10^{13}$ cm^{-2} and 0, respectively. (d)-(f) Cut-line $J_{electron}$ under the depths of 0.001, 1 and 10 μm, respectively.

3.4.4 Conclusion

The surface passivation mechanism of the Si substrate by the electric field induced by charges inherent to the dielectric films has been clarified through numerical simulations. The impact of device properties on IBC SCs has been investigated, revealing that surface fixed charges suppress interface carrier recombination by inducing energy band bending at the Si surface. The relationship between Q_f at the rear gap surface, S_{gap}, and *PCEs* of IBC SCs has been examined, showing that high device performance with outstanding *PCE* can be achieved for cases with a high-level $|Q_f| > 10^{12}$ cm^{-2} or a low-level $|Q_f| < 10^{11}$ cm^{-2}. The simulations also indicate that cases with positive fixed charges exhibit higher *PCE* than cases with negative fixed charges if $|Q_f|$ is less than 2×10^{11} cm^{-2}, but cases with negative fixed charges can achieve excellent *PCE* if $|Q_f|$ is larger than 5×10^{11} cm^{-2}. Shrinking the rear gap size (f_{gap}) can promote the *PCE* of this type of IBC-HJ SC with poor gap passivation ($S_{gap} = 10^3$ cm/s), but it may not completely suppress carrier recombination losses even if f_{gap} is small enough. The

distributions of electric field and carrier current density have been further examined to reveal the carrier transport channel. The simulations also indicate that the fixed charges in the gap region can affect the passivation quality of other related interfaces (ETL and front surface) in the case of poor passivation. Specifically, for weak ETL passivation with S_{ETL} of 10^3 cm/s, the case of $Q_f = -10^{13}$ cm^{-2} has a positive effect on cell performance, while positive fixed charges are almost ineffective. Additionally, the case of negative fixed charges in the rear gap with high Q_f also shows a high tolerance to f_{ETL} and *pitch* size. In the case of poor passivation at the front surface with S_{front} of 100 cm/s, the cases of $Q_f = \pm 10^{13}$ cm^{-2} can enhance cell performance, especially for thin Si wafers that are susceptible to the influence of rear gap fixed charges. The presented results and passivation mechanism provide a simple and feasible approach for the development of high-efficiency IBC SCs.

Chapter 4 TOPCon Solar Cells

4.1 Synopsis

TOPCon solar cells are emerging as a promising technology in the field of photovoltaics, offering significant advantages in terms of module costs and cell efficiencies. One of the key structures in TOPCon solar cells is an ultra-thin SiO_x film covered by a heavily doped poly-Si layer, which serves the dual purpose of providing high-quality passivation to Si substrates and acting as a carrier selective transport layer, inducing band bending at the c-Si surface. To date, high-efficiency TOPCon solar cells have been achieved, with the high reported efficiencies of 26.0% and 26.1% by Fraunhofer ISE,[139] and by ISFH[18,140] for a normal structure and IBC design, respectively. However, further enhancing the efficiency of TOPCon devices poses challenges due to a lack of understanding of the underlying physical mechanisms governing carrier transport. Specifically, the mechanism of carrier transport through the poly-Si/SiO_x/c-Si contact is not yet fully comprehended.

Regarding this junction, two distinct narratives exist. Some believe that carriers are primarily transported through the SiO_x layer *via* tunneling, while others argue that carriers are predominantly transported through pinholes. It is well-known that carriers can easily tunnel through a SiO_x thin film if the SiO_x layer is less than 1.7 nm thick, but tunneling becomes difficult when the SiO_x layer exceeds 2 nm in thickness. In the former case, carrier transport can be explained by the classical tunneling theory.[141] However, evidence suggests that high-efficiency TOPCon solar cells can still be achieved even when the SiO_x thickness reaches 2 nm, indicating that the classical tunneling model has limitations in explaining this phenomenon. On the other hand, from the pinhole perspective, carrier transport through thicker SiO_x films relies more on pinholes.[142] Additionally, the size and density of pinholes, which can be controlled by annealing conditions, also impact carrier transport. Moreover, for thin SiO_x layers

with pinholes, both tunneling and pinhole-mediated transport mechanisms may coexist. Therefore, further investigation is necessary to determine the transport mechanism for this junction, whether it involves carrier transport through pinholes or direct tunneling.

In this chapter, well-designed experiments and simulations were conducted to understand the intrinsic dynamics of the poly-Si/SiO_x/c-Si design with pinholes in the local region. The measurements included the process of pinhole formation and the mechanism of charge carrier transport.

4.2 Measurement and Characterization

4.2.1 Measurement Methods

For the measurements of passivation quality, contact resistance, transmission electron microscopy (TEM), and electrochemical capacitance-voltage (ECV), *n*-Si wafers with a resistivity of approximately 3 Ω·cm and a thickness of 170 μm were used. The conductive Atomic Force Microscopy (c-AFM) measurement utilized double-polished c-Si wafers. The passivation properties of devices including implied open-circuit voltage (iV_{oc}) and recombination current (J_0) were extracted using a Sinton lifetime tester (WCT-120) with the Quasi-Steady-State-Photoconductance (QSSPC) method. Doping distributions were obtained through an ECV measurement system (Buchanan, CVP21). Contact resistivity was measured using Cox and Strack method. For the samples used for contact measurement, the metal dots with different diameters (*i.e.*, 0.3, 0.6, 0.8, 1.0, 1.2, 1.6, 1.8, 2.0, and 2.4 mm) were thermally evaporated through shadow masks on the front side of samples, and a whole area electrode was formed by GaSn paste on the rear-side of samples. TEM samples prepared by focused ion beam (FIB) were analyzed using Talos F200X. The c-AFM measurement was performed using the Dimension ICON SPM platform.

4.2.2 TEM Measurement

Figure 4.1 shows the confirmation of SiO_x quality and the presence of pinholes through TEM measurements. The morphology of the SiO_x layer was partly determined by the subsequent annealing process.[143] The research focused on samples subjected to varied annealing temperatures (T_a). Three typical T_a values were considered: 760℃, 820℃, and 950℃. Here, it is important to mention that the samples used for TEM measurement were prepared by Dr. Zunke Liu.

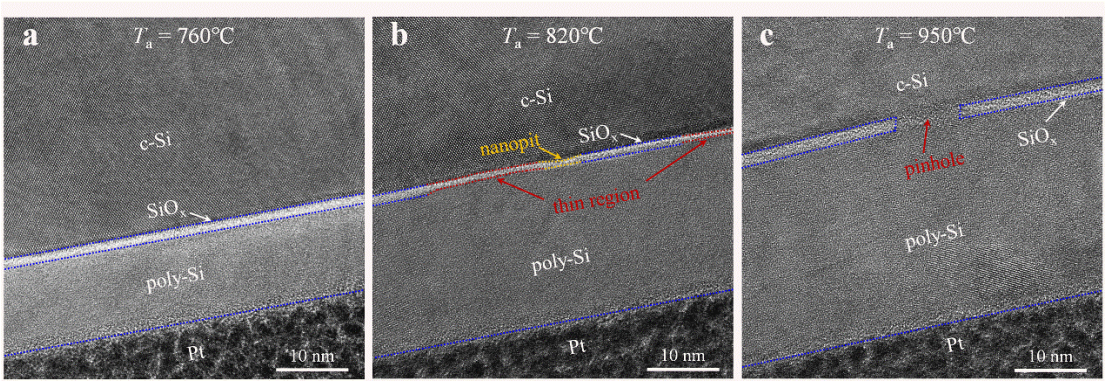

Figure 4.1 (a)-(c) TEM maps for poly-Si/SiO_x/*n*-Si structure under the various T_a with a 10 nm scalebar.

For comparison purposes, large-scale TEM maps of the three samples were also illustrated in **Figure 4.2**. **Figure 4.1**a clearly shows that for T_a = 760℃, a perfect SiO_x film with a uniform thickness of approximately 1.7 nm was obtained. This indicates that the SiO_x layer is resistant to breaking when the annealing temperature is relatively low. In **Figure 4.1**b, for T_a = 820℃, the SiO_x thickness shows no significant variation, but nanopits and thin regions can be observed at local positions along the SiO_x interface, suggesting that the SiO_x film undergoes slight destruction during annealing at a moderate temperature. In **Figure 4.1**c, for T_a = 950℃, the SiO_x layer is severely damaged with the emergence of pinholes, resulting in direct contact between the *n*-Si substrate and the poly-Si layer.

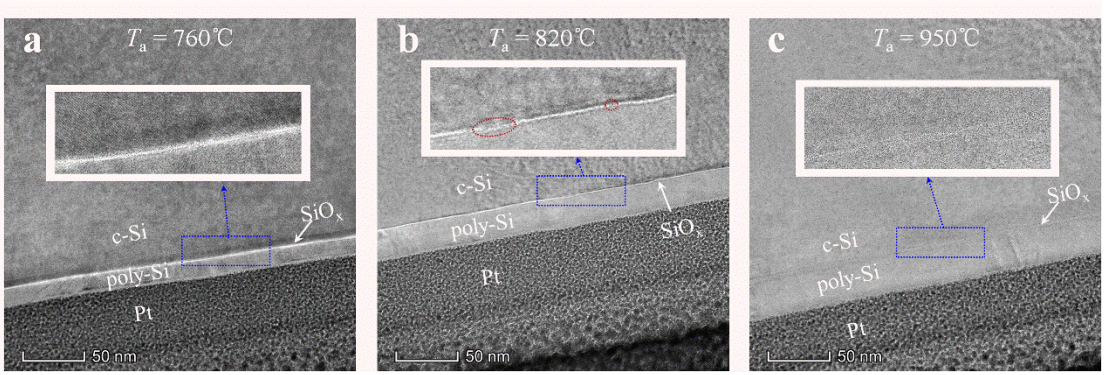

Figure 4.2 (a)-(c) TEM maps for poly-Si/SiO_x/*n*-Si structure under the various T_a with a 50 nm scalebar.

To further evaluate the impact of T_a on the SiO_x layer, EDS measurements were conducted. **Figure 4.3** illustrates that the intensities of O/Si signals decrease as the temperature of T_a increases from 760°C to 950°C, corroborating the findings from the TEM images.

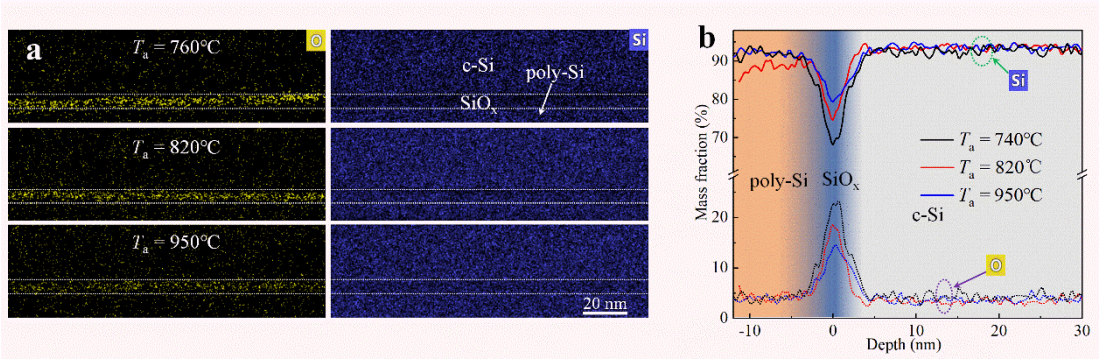

Figure 4.3 (a) EDS and (d) mass fraction as a function of depth for Si and O elements.

4.2.3 c-AFM Measurement

The TEM results presented in **Figure 4.1** provide information only about the local SiO_x region. To investigate the pinhole density (D_{pin}) over a larger area, the c-AFM method was employed, as depicted in **Figure 4.4**. Here, it is important to mention that the samples used for c-AFM measurement were prepared by Mei Cui. In this method, the conductive current is predominantly transported through pinholes while being restricted within the SiO_x section.

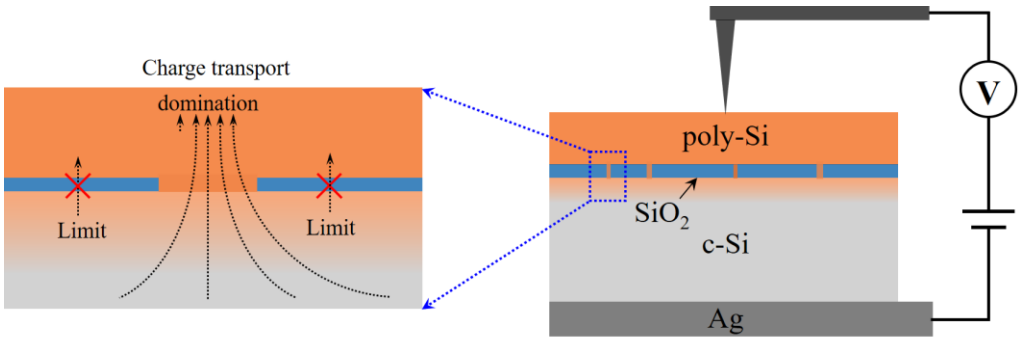

Figure 4.4 Sketch map for c-AFM measurement.

Experimental results are shown in **Figures 4.5** and **4.6**, indicating that the current improved with the emergence of more hotspots as T_a increased from 760°C to 950°C. To facilitate comparison, the corresponding current statistics are presented in **Figures 4.5**d-**4.5**f, demonstrating enhanced current intensities for higher T_a values. Specifically, samples subjected to T_a temperatures of 760°C/820°C/950°C exhibited D_{pin} values of $7.2\times10^7/3.1\times10^8/2.0\times10^9$ cm^{-2}, respectively.

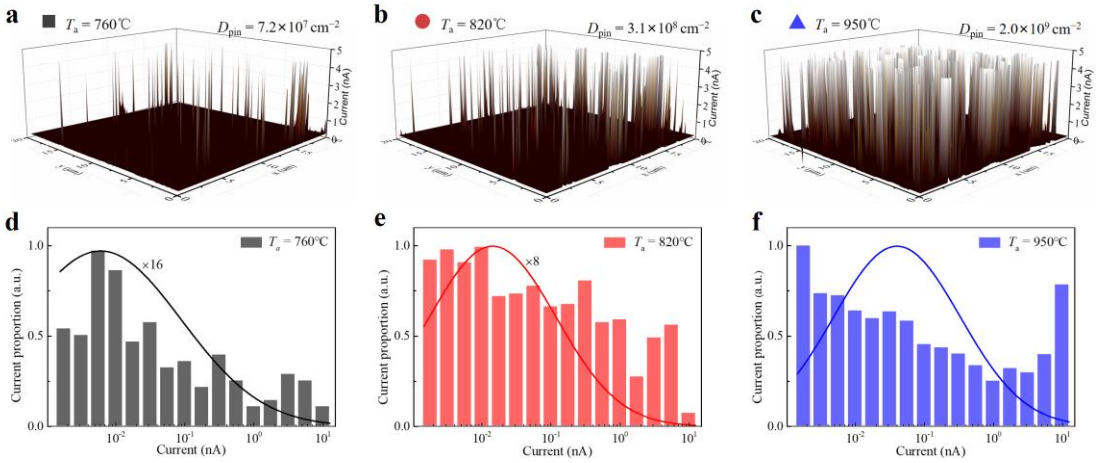

Figure 4.5 (a)-(c) 3D current distributions. (d)-(f) The corresponding current statistics for the three related cases.

Here, the pinhole density values for samples under different annealing temperatures (760°C/820°C/950°C) were calculated using a statistical method. In this method, the presence of pinholes is identified by analyzing the high current responses observed in the conductive atomic force microscopy (c-AFM) measurements. By counting the

number of high current responses within a specific test area, the pinhole density can be determined. The calculated pinhole density values for the three respective annealing temperatures were found to be 7.2×10^{7} cm^{-2}, 3.1×10^{8} cm^{-2}, and 2.0×10^{9} cm^{-2}.

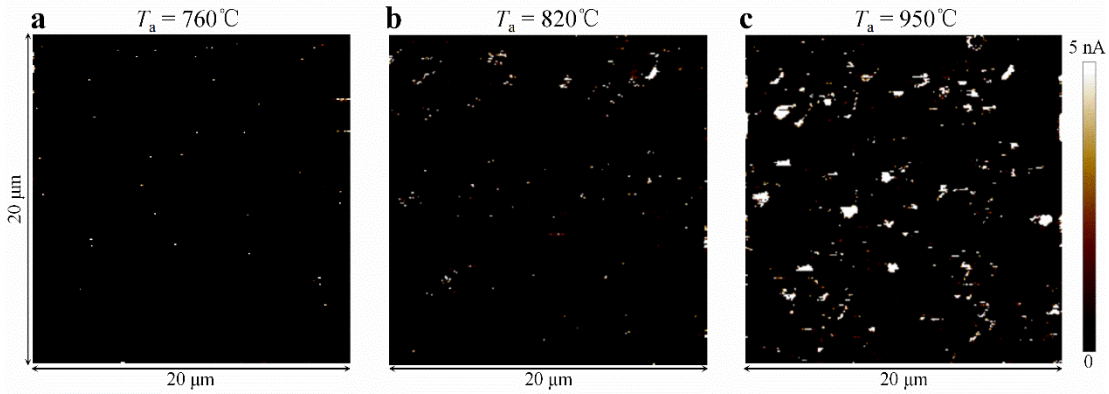

Figure 4.6 2D current distributions for the three related cases.

Additionally, **Figure 4.7** showcases the statistical D_{pin} distributions of this study as well as other approaches, including c-AFM [144-146], TEM[147], and SEM[148-150]. The latter two methods have significant limitations; TEM, although capable of accurately determining pinhole size, is restricted to local measurement regions, while SEM magnifies pinhole size through selective etching of the c-Si substrate, leading to underestimated D_{pin} values. Despite the limitations of the c-AFM method, such as potential overestimation of small pinhole sizes due to the relatively large size of the c-AFM tip (tens of nanometers) and possible lateral current conductivity in the poly-Si film, it is considered a suitable approach at this stage. It should be noted that the measured currents in c-AFM measurements may be influenced by the textured surface, as illustrated in **Figure 4.8**. However, for flat samples, the measured currents effectively reflect information about the SiO_x interface.

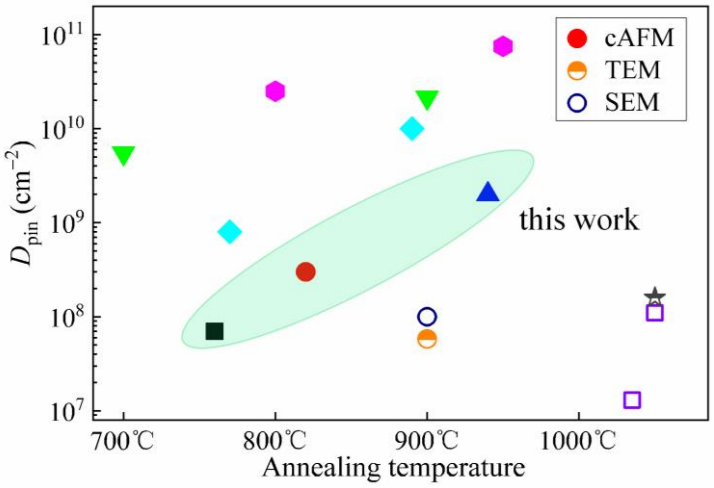

Figure 4.7 D_{pin} distributions under the various annealing temperatures.[144-150]

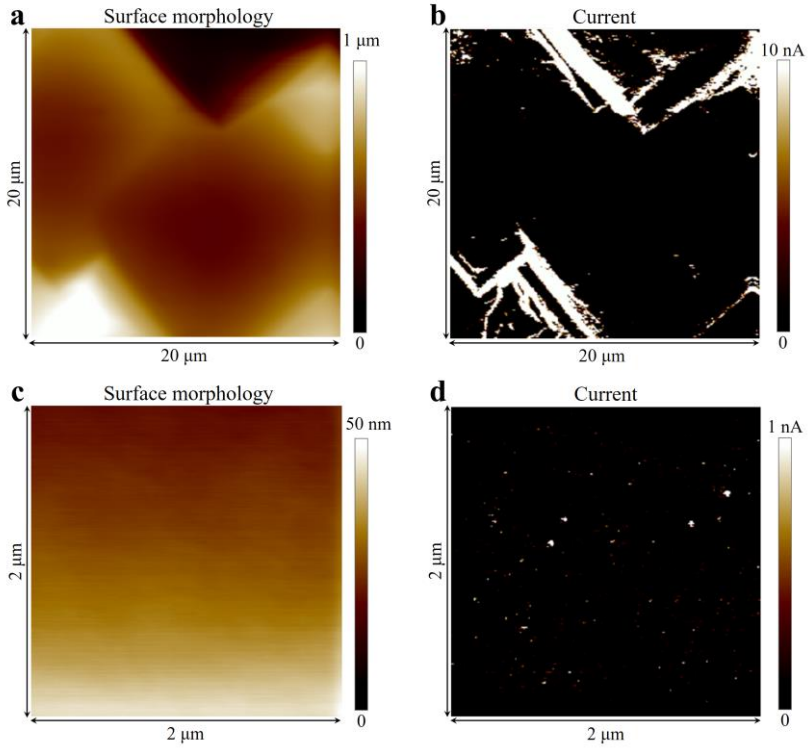

Figure 4.8 (a)/(c) Surface morphologies, and (b)/(d) the corresponding current distributions for the random structured/flat samples.

4.3 Pinhole Formation Mechanism

4.3.1 Theory Investigation

Although the existence of pinholes has been confirmed through TEM measurements, the exact process of pinhole formation remains unclear. Several potential mechanisms have been proposed to address this issue.[151-155] Firstly, one possible mechanism involves the local region's destruction of the SiO_x layer through the reaction of Si and SiO_x, resulting in the formation of volatile SiO.[151,153-155] However, this model has been challenged by some researchers who argue that it requires an open interface for the products to escape, which contradicts the fact that polysilicon coatings on SiO_x films do not prevent pinhole formation during high-temperature annealing.[152]

The second proposed mechanism is the viscous-flow model. The viscoelastic relaxation within the SiO_x layer can alleviate compressive stresses, especially in samples subjected to high-temperature processes.[156] Carim also presented a model that considers the effects of stress and viscous flow, which explains the experimental observations that high-temperature annealing reduces surface roughness. According to this model, stress relief through viscous flow can result in a smoother surface, indicating that this mechanism does not support pinhole formation.[157]

The third model suggests that initial voids are formed due to tensile stresses resulting from the thermal expansion coefficient differences between the oxide layers and c-Si substrates.[158] Additionally, intrinsic stresses arising from differences in thermal expansion coefficients can be alleviated through viscoelastic relaxation.[159] More likely, these models exist simultaneously and compete with each other. In cases where the temperature is not very high (< 1000ºC), i prefer the theory of thermal stress here.

4.3.2 Pinhole Formation Process

Understanding the mechanisms of pinhole formation under various annealing processes is crucial since pinhole formation is greatly influenced by the annealing process. In order to clarify the relationship between annealing process and pinhole formation, well-designed experiments were conducted under different annealing conditions, including control annealing and rapid heating/cooling. The normal annealing process is depicted in **Figure 4.9**.

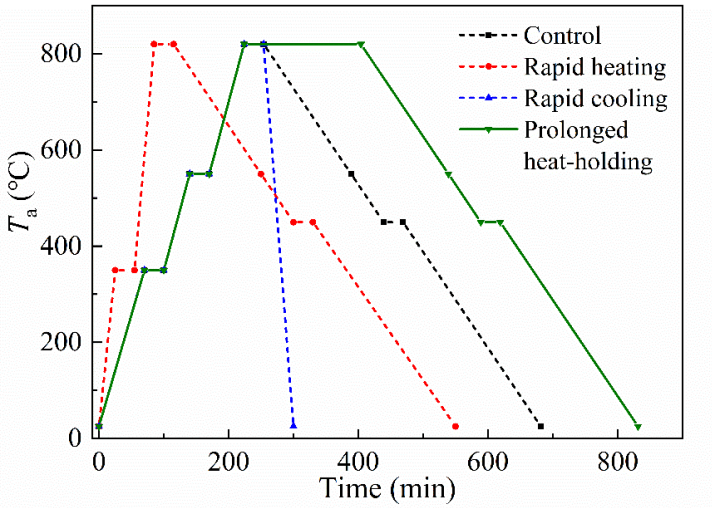

Figure 4.9 Time-dependent annealing process.

Figures 4.10 and **4.11** reveal that for the case of T_a = 820°C, the rapid annealing process increases the pinhole density (D_{pin}) from 3.2×10^8 cm^{-2} in the control case to $7.0\times10^8/1.7\times10^9$ cm^{-2} in the rapid heating/cooling case, respectively. Although rapid annealing reduces the process time, it leads to an increase in pinhole density, indicating that the ramping rates of anneal temperatures have a significant impact on pinhole densities, surpassing the influence of anneal times. Additionally, pinholes can be formed during the heating and/or cooling stages. Rapid annealing can result in the degradation of the SiO_x film due to stress deformation caused by thermal expansion. Furthermore, the effect of increased heat-holding time at the temperature-plateau on device performance was investigated. **Figure 4.11** demonstrates that an insignificant

improvement in pinhole densities was observed with the increase in heat-holding time for both 820°C and 950°C annealing, with values of $3.2\times10^{8}/3.5\times10^{8}$ cm^{-2} to 2.0×10^{9} $cm^{-2}/2.1\times10^{9}$ cm^{-2} for control/prolonged cases, respectively. This suggests that prolonging the heat-holding time under the temperature-plateau does not accelerate the degradation of the SiO_x layer, leading to the abandonment of the high reaction and viscous flow models in this study.

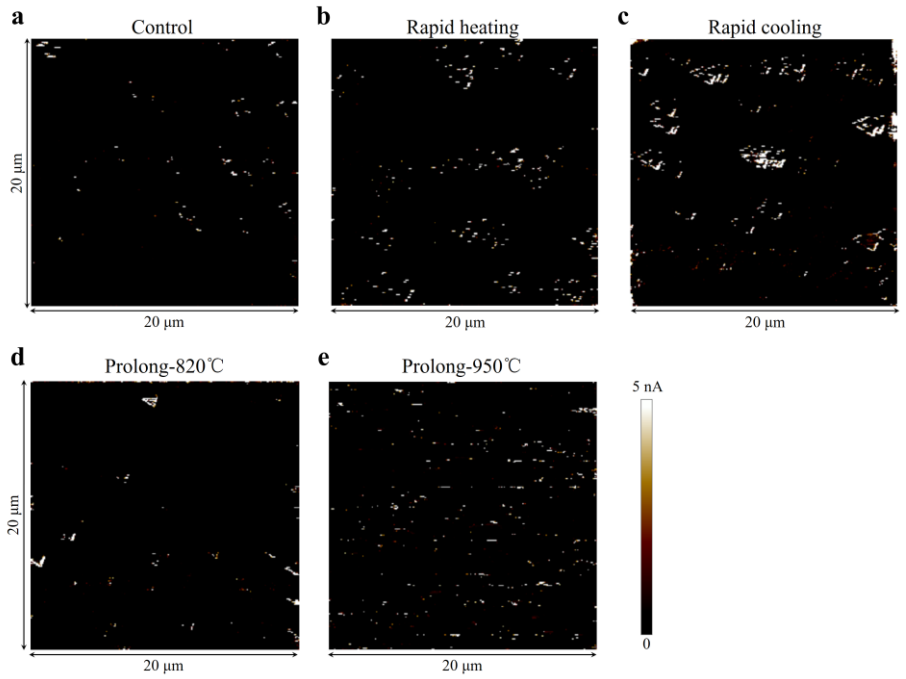

Figure 4.10 2D current distributions by c-AFM measurements under the various annealing processes.

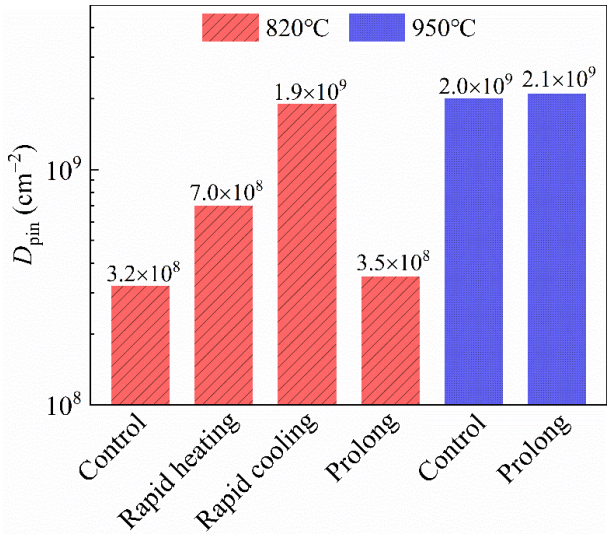

Figure 4.11 D_{pin} distributions under the various annealing conditions.

To validate the mechanisms of pinhole formation, a physical model was proposed, as depicted in **Figure 4.12**. This simplified model does not consider the initial residual stress resulting from film deposition. During the heating process, all films, including SiO_x, poly-Si, and Si substrate, expand. As shown in **Figure 4.13**a, Si and poly-Si have higher thermal expansion coefficients (α) compared to SiO_x. Consequently, the poly-Si films and Si substrates experience greater extension than the SiO_x film, resulting in compressive and tensile stresses in the Si substrate and SiO_x film, respectively. The tensile stresses in the SiO_x film increase with higher anneal temperatures. Due to the thinness of the SiO_x film, the accumulated stresses within it can cause the film to fracture. This fracture partially relieves the film deformation, releasing stress within the SiO_x film and Si substrates.

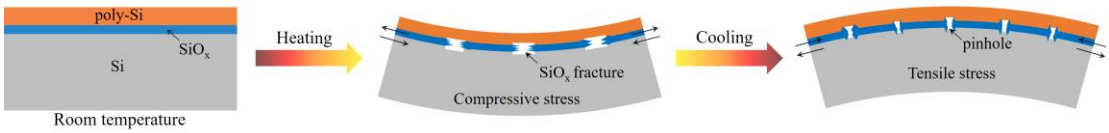

Figure 4.12 Process of pinhole formation.

The cooling process is the reverse of the heating process. As the temperature decreases, all films undergo compression, but the Si substrate and poly-Si film experience greater

compression, resulting in tensile/compressive stresses in the Si/SiO_x layers. Similarly, the external deformation caused by differences in thermal expansion during the cooling process can be expected, which can be alleviated by facilitating SiO_x fracture, thereby leading to pinhole formation. In high-temperature annealing processes, the deformation and stress in SiO_x films are typically alleviated or released through SiO_x film fracture, indicating that more pinholes suggest less stress.

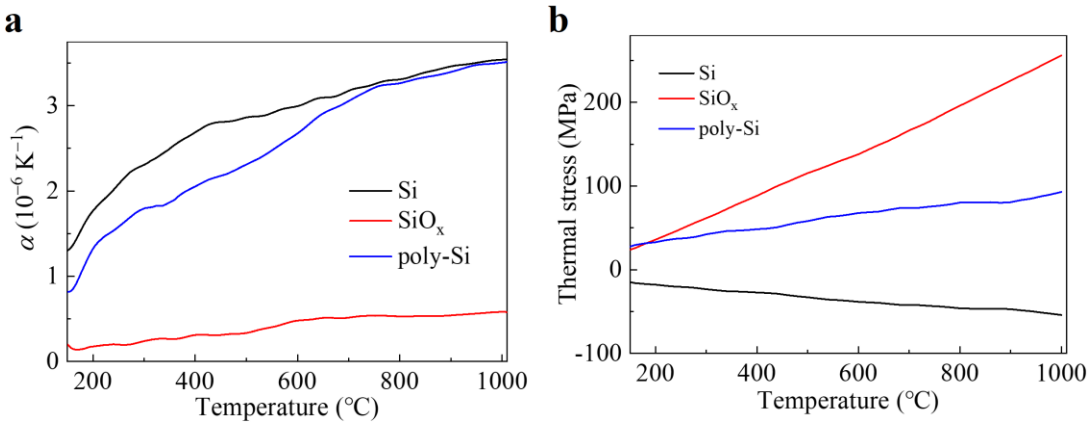

Figure 4.13 (a) Thermal expansion coefficients (α) under the various temperatures. (b) The simulated thermal stresses of the poly-Si and SiO_x films as well as Si surfaces under the various temperatures.

To support this conclusion, a theoretical model was developed to establish the correlation between deformation and thermal stress. The related numerical simulation parameters are presented in **Table 4.1**. As depicted in **Figure 4.13**b, there is an increasing trend in stresses across all layers with temperature variation. In the SiO_x layer, high stress at elevated temperatures is likely responsible for pinhole formation.

Table 4.1 Parameters used for thermal expansion simulation.

Material parameters	Si	SiO_x	Poly-Si
Young's modulus, E (Pa)	1.7×10^{11}	0.731×10^{11}	1.69×10^{11}
Poisson's ratio, μ	0.28	0.17	0.22
Density, ρ (kg/m^3)	2329	2200	2320

Furthermore, spatial distributions of deformations and stresses during the heating stage were demonstrated in **Figure 4.14**. It is evident that stress accumulation near the SiO_x layer can be observed, which can be relieved in the case of pinholes. It is important to note that pinhole formation is a complex process involving the simultaneous occurrence of various mechanisms. Apart from SiO_x thickness, the deposition approaches of SiO_x can lead to different densities and homogeneity, which may significantly affect the optimal annealing conditions.[160]

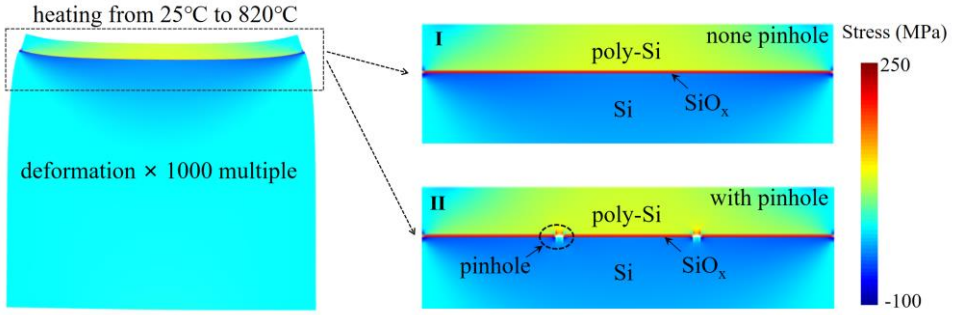

Figure 4.14 Spatial distributions of deformations and stresses for the poly-Si/SiO_x/c-Si contacts.

4.4 Carrier Transport Mechanism

4.4.1 Tunneling & Pinhole Current

To further confirm the carrier transport mechanism in poly-Si/SiO_x/*n*-Si contacts, specifically whether it is dominated by pinholes or tunneling, transport currents through SiO_x tunneling and pinholes were investigated.

Using a poly-Si(*n*)/SiO_x/*n*-type Si junction as an example, numerical simulations were conducted with the electrical parameters listed in **Table 4.2**. The simulation details were demonstrated in Chapter (2.3 Thermal Stress).

Table 4.2 Electrical parameters used for simulations.

Material parameters	Si	SiO_x	poly-Si	Si(p^+)
Thickness, μm	180	0.0017	0.04	ECV dep.
Electron affinity, χ (eV)	4.05	0.9	4.05	4.05
Bandgap energy, E_g (eV)	1.12	9	con. dep. bgn	con. dep. bgn
Relative dielectric permittivity, ϵ_r	11.7	3.9	11.7	11.7
Effective conduction band density, N_c (cm^{-3})	2.8×10^{19}	/	2.8×10^{19}	2.8×10^{19}
Effective valence band density, N_v (cm^{-3})	1.04×10^{19}	/	1.04×10^{19}	1.04×10^{19}
Doping concentration, N_d or N_a (cm^{-3})	2.3×10^{15}	/	ECV dep.	ECV dep.
Mobility of electron/hole, μ_n/μ_p (cm^2/Vs)	con. dep.	/	con. dep.	con. dep.
SRH life time, τ_n/τ_p (ms)	10	/	0.01	0.01
Radiative recombination coefficient, C_{Rad} (cm^3s^{-1})	9.5×10^{-15}	/	9.5×10^{-15}	9.5×10^{-15}
Auger recombination coefficient, A_n/A_p (cm^6s^{-1})	$2.8/0.99\times10^{-31}$	/	$2.8/0.99\times10^{-31}$	$2.8/0.99\times10^{-31}$
Electron/hole tunneling mass	/	0.35/0.35 m_0	/	/

Figure 4.15 illustrates the tunneling current fractions under various pinhole

densities/sizes and SiO_x thicknesses. The results suggest the following: 1) With an increase in D_{it} (interface trap density), tunneling currents decrease while currents through pinholes increase. 2) Larger pinhole size (W_{pin}) promotes pinhole currents. 3) Charge carriers in thin SiO_x layers are more likely to transport via tunneling behavior. 4) Charge carriers in thick SiO_x layers are more likely to transport through pinholes.

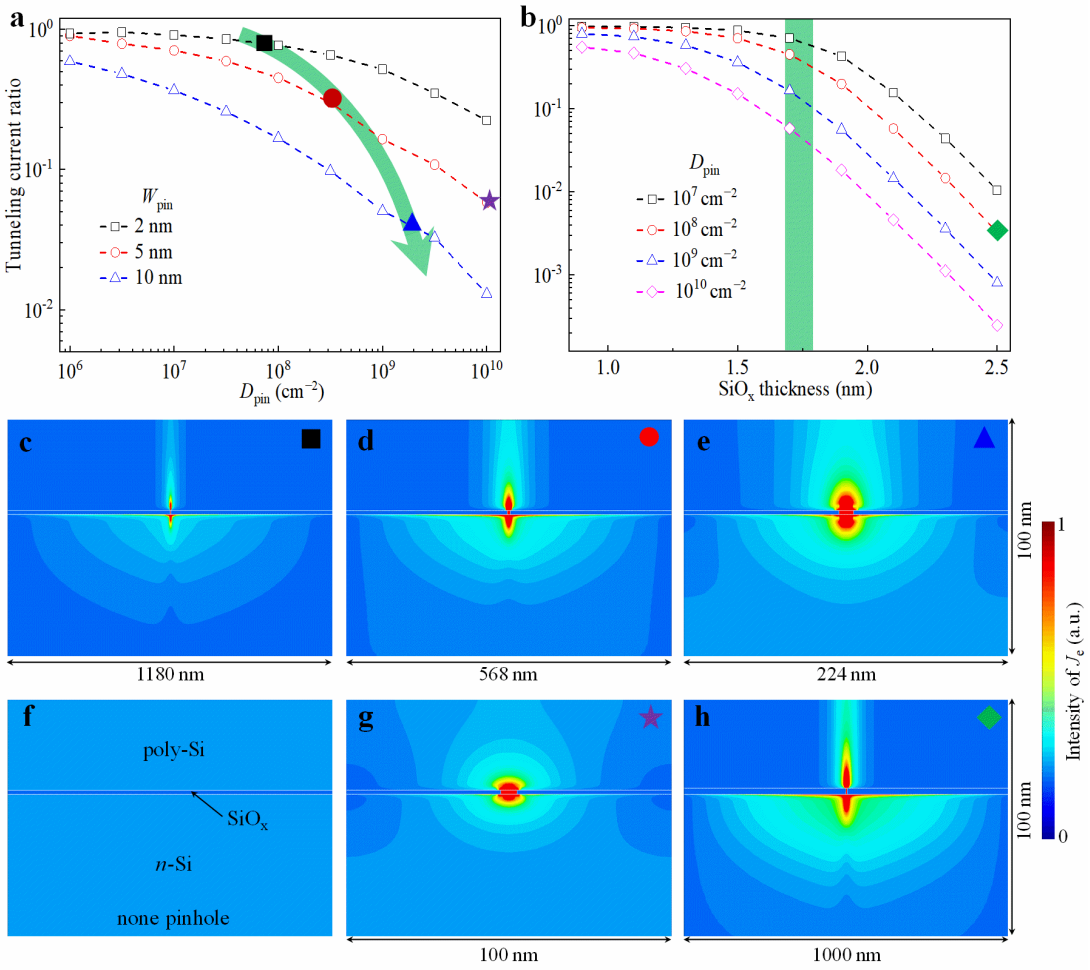

Figure 4.15 Tunneling current fractions under the various (a) D_{pin} and (b) SiO_x thickness. (c)-(h) The corresponding profiles of electron currents of poly-Si/SiO_x/*n*-Si design.

Specifically, **Figure 4.15**a highlights representative samples subjected to high-temperature annealing, indicating a change in the transport mechanism from tunneling-dominant to pinhole-dominant behavior. To further validate these conclusions, profiles of electron currents under representative cases were examined. **Figure 4.15**f shows that in the absence of pinholes, the electron current exhibits a uniform distribution along the

lateral direction. However, with the introduction of pinholes, electrons accumulate near the pinhole region, forming hotspots of electron currents, indicating a direct channel for electron transport through pinholes. In summary, these simulation results quantify the tunneling and pinhole transport currents under different SiO_x thicknesses, pinhole densities, and sizes. The dominant mechanism depends on factors such as pinhole density/size and SiO_x thickness.

4.4.2 Passivation and Contact Properties

For poly-Si/SiO_x/*n*-Si contacts, the presence of pinholes significantly affects the passivation and contact properties. **Figure 4.16** displays the contact resistivity (ρ_c) and iV_{oc} measurement under various annealing conditions to elucidate the impact of annealing on the contact and passivation performance. Here, it is important to mention that the *ECV*, ρ_c and iV_{oc} measurements were conducted by Dr. Zunke Liu.

In the case of *n*-type poly-Si, high-temperature annealing facilitates the diffusion of P impurities into the *n*-Si substrate, resulting in an in-diffused region on the *n*-Si surface. **Figure 4.16**a shows that the annealing temperature directly affects the diffusion depth and concentration of P impurities. Specifically, as T_a increases, the diffusion depth and concentration were increased. The contact properties, as depicted in **Figure 4.16**b, indicate that the contact resistivity of this junction decreases with increasing annealing temperature, with values of 72.1/15.4/9.9/6.7 $m\Omega \cdot cm^2$ for T_a = 760°C/820°C/900°C/950°C. This implies that higher annealing temperatures contribute to lower contact resistivities. The original *I-V* curves for calculating the contact resistance were displayed in **Figure 4.17**. The passivation properties of this junction, shown in **Figure 4.16**c, exhibit an increasing and then decreasing trend as T_a increases from 760°C to 950°C, with the best passivation observed at T_a = 820°C. In detail, the four representative samples yield an iV_{oc} of 723/736/724/661 mV for T_a = 760°C/820°C/900°C/950°C.

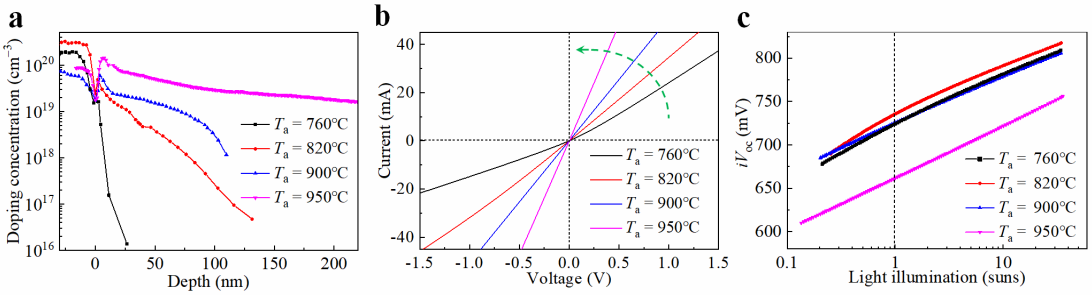

Figure 4.16 (a) Profiles of doping concentrations, (b) *J*-*V* curves in dark, (c) iV_{oc} under the various light intensities from experiments for the four representative T_a.

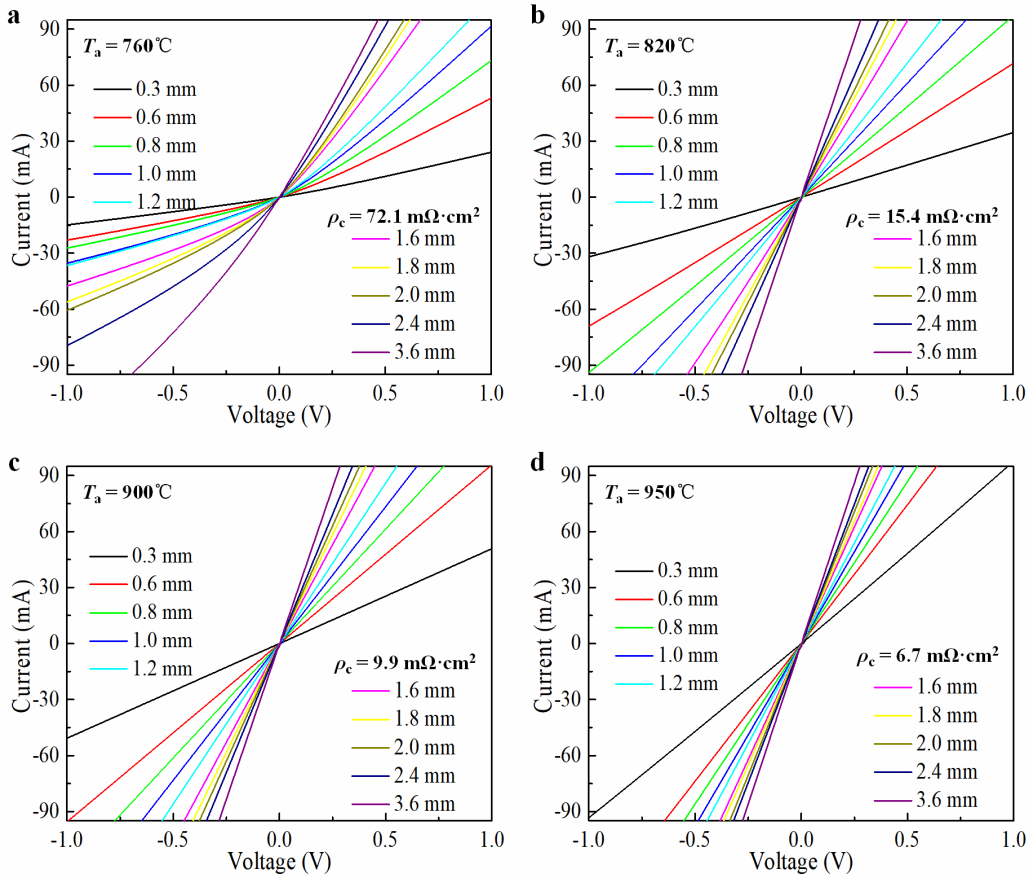

Figure 4.17 Measured *J*-*V* curves in dark under the different T_a.

It is important to note that the passivation performance of the poly-Si/SiO_x/*n*-Si contact relies on the combined contributions of in-diffused electric-field passivation and pinhole mediation, with annealing treatment playing a crucial role. The in-diffusion doping caused by high-temperature annealing is necessary to induce a strong electric field, which provides the passivation effect. The positive induced electric field reduces

charge-carrier recombination by accelerating majority carrier transport.

While the in-diffused doping can enhance certain aspects, it also introduces challenges such as increased Auger and/or SRH recombination. This is especially significant when dealing with in-diffused profiles that have high concentration and/or depth. In order to verify these conclusions, numerical simulations were conducted to examine the passivation properties. The simulation details were demonstrated in Chapter 2 (2.2 Passivation and Contact Properties). **Figure 4.18** illustrates that the passivation properties decrease as $D_{\text{it-pinhole}}$ (the interface defect density of the pinhole region) increases. The best passivation is achieved by considering both the recombination loss and the electric-field passivation resulting from the presence of the in-diffused profiles. Additionally, high-temperature annealing treatments can accelerate the degradation of SiO_x, leading to more defects in the interface and inferior-level passivation.

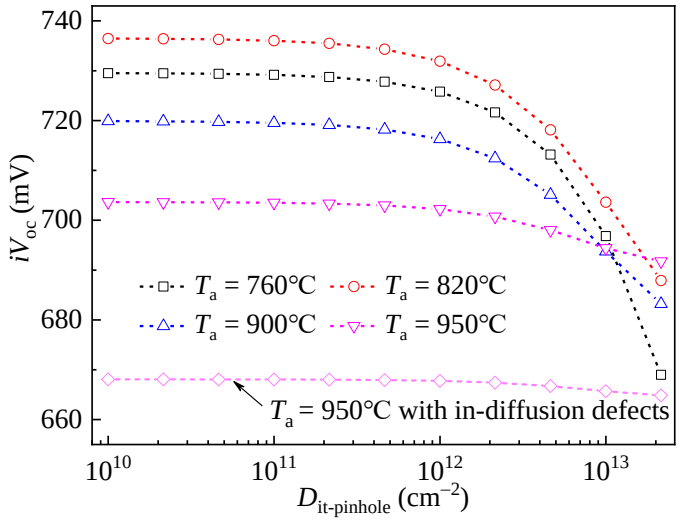

Figure 4.18 Simulated iV_{oc} under the various $D_{\text{it-pinhole}}$.

Although the impact of annealing temperature on device performance has been discussed, it lacks broad applicability. It is necessary to establish a fundamental physical model to elucidate the relationship between passivation/contact performance and pinholes. **Figure 4.19** clearly shows that the transport currents consist of four components: majority/minority carrier current across the pinhole ($J_{\text{maj,pin}}$/$J_{\text{min,pin}}$) and

oxide ($J_{maj,tun}/J_{min,tun}$). For the case without SiO_x, a high recombination is expected due to the high interface states at poly-Si/Si interface, leading to a high $J_{min,pin}$; for the case with SiO_x, the recombination loss is reduced because of the lower interface states at SiO_x/Si interface, which thus result in a low $J_{min,tun}$.

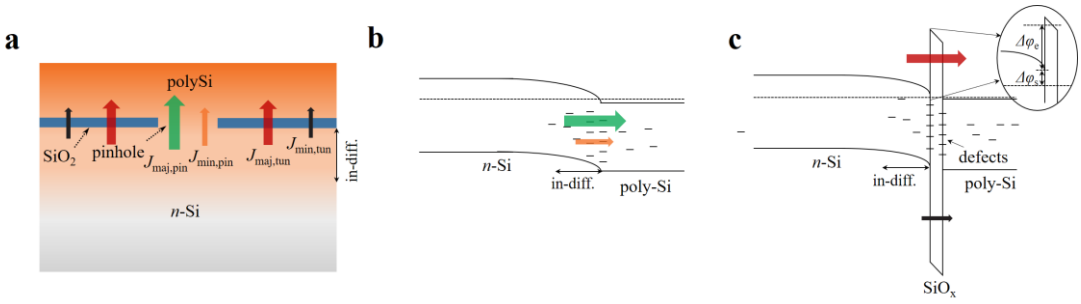

Figure 4.19 (a) Diagram of current transport for poly-Si/SiO_x/*n*-Si contact featuring pinholes. The corresponding energy-band diagrams without (b) and with (c) SiO_x.

Specifically, **Figure 4.20** reveals that as D_{pin} increases, $j_{0,tun}$ and $\rho_{c,tun}$ remain constant, while $j_{0,tun}$ exhibits a decreasing trend and $\rho_{c,tun}$ shows an increasing trend. This results in a reduced/increased variation for ρ_c/j_0. Furthermore, the experimental data points align with the simulated results, except for T_a = 820°C.

To evaluate passivation and contact performance simultaneously, the selectivity factor defined in Chapter 2 was investigated. As depicted in **Figure 4.20**c, a high *S* value approaching 15 is observed for T_a = 820°C, a moderate *S* for T_a = 760°C and 900°C, and a poor *S* for T_a = 950°C. Moreover, the figure highlights related data points reported by others,[161-166] suggesting the possibility of achieving a remarkable *S* value exceeding 16.

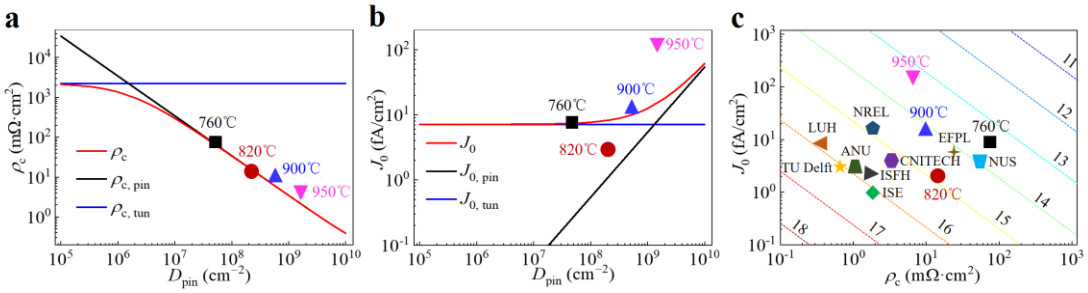

Figure 4.20 (a) Simulated ρ_c and (b) J_0 under the various D_{pin}, where the typical cases under the different temperature annealing treatment were marked in the figure. (c) Selectivity factors under the various ρ_c and J_0.

4.5 Device Performance

4.5.1 Device Fabrication Process

An industrially cell-manufacturing process was utilized for the production of the TOPCon solar cells. The wafers used were Czochralski grown (Cz) phosphorus-doped *n*-type mono-crystalline silicon, which have a resistivity of ~1 Ω·cm, a size of 156×156 mm^2, and a thickness of ~170 μm. The surface of the wafers underwent conventional alkaline texturing using a KOH solution with organic additives. A boron-diffused region was then created in a tube furnace using a BBr_3 source. Subsequently, an industrial single side etching process with HF/HNO_3 was employed to remove the diffused layers on the rear side. The doping profile of the front-sided B concentration was illustrated in **Figure 4.21**, which was measured using ECV.

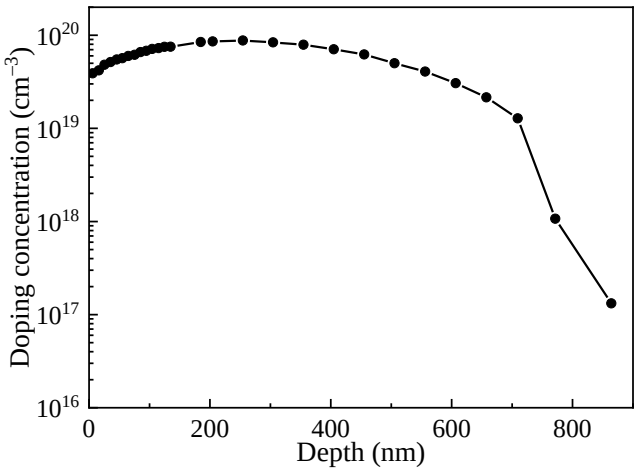

Figure 4.21 Measured front-sided P^+ doping profile.

Following these steps, a thin layer of thermal oxide was grown on the rear side. Intrinsic poly-Si deposition took place using low-pressure chemical vapor deposition (LPCVD) at a temperature of 550°C. The intrinsic poly-Si was doped through a $POCl_3$ diffusion furnace to form n^+ poly-Si with a thickness of ~150 nm. Annealing treatments were performed within a temperature range of 760°C to 950°C to facilitate P diffusion and prepare the n^+ poly-Si. Subsequently, a single-side KOH etch process at 60°C was

employed to remove the wrap-around poly-Si on the front side. The front side was then passivated and provided with an anti-reflection coating (ARC) using atomic layer deposition (ALD) SiO_x and Al_2O_3, capped with plasma-enhanced chemical vapor deposition (PECVD) SiN_x. The rear poly-Si structure also received ALD SiO_x and PECVD SiN_x capping. Lastly, Ag/Al and Ag pastes were screen-printed and co-fired in a belt furnace to form the front and rear contact grids, respectively. Both the front and rear metal contact grids had a finger spacing of 1.4 mm and a bus bar spacing of 6.37 mm.

4.5.2 Device Performance

In this section, the complete TOPCon SCs with poly-Si/SiO_x/*n*-Si contacts on the rear side were presented. Here, it is important to mention that the TOPCon devices were fabricated by Jolywood. The proof-of-concept TOPCon SCs, as shown in **Figure 4.22**, have an effective area of 156×156 mm^2.

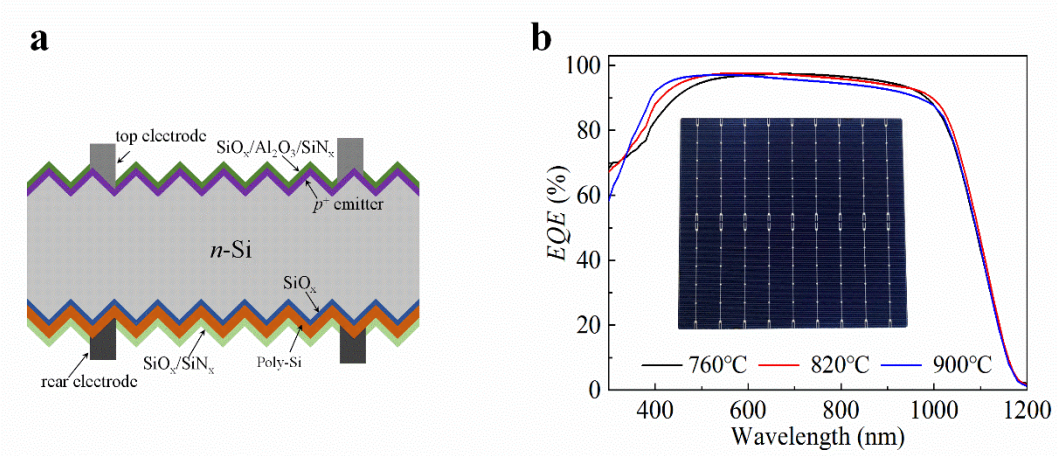

Figure 4.22 (a) Schematic diagram of TOPCon SCs. (b) *EQE* spectra for the three-typical cases.

Figure 4.23 and **Table 4.3** display the electrical parameters of TOPCon SCs at different annealing temperatures (T_a) of 760°C, 820°C, and 900°C. It is evident that with increasing T_a, the *FF* improves due to decreased contact resistivity. The cases with T_a

of 820℃ exhibit the highest V_{oc} due to superior passivation quality. Overall, samples annealed at T_a = 820℃ achieve high *PCE* values (> 23.5%), which are higher than the *PCE* values of 22.5% and 22.7% for T_a = 760℃ and T_a = 900℃, respectively. Additionally, the external quantum efficiency (*EQE*) spectra for the three cases were demonstrated in **Figure 4.22**b. It is known that high-temperature annealing could only change the characteristics of the back side polycrystalline silicon, which theoretically does not affect the quantum efficiency of the short band. Therefore, it is speculated that the differences in *EQE* in the short band may be caused by the thickness of the antireflection layer in different batches.

Table 4.3 Electrical parameters of TOPCon SCs from experiments.

Samples	J_{sc} (mA/cm^2)	V_{oc} (V)	*FF* (%)	*PCE* (%)
760℃	40.97	0.698	78.91	22.56
820℃	40.92	0.704	81.48	23.49
900℃	40.63	0.685	81.77	22.76

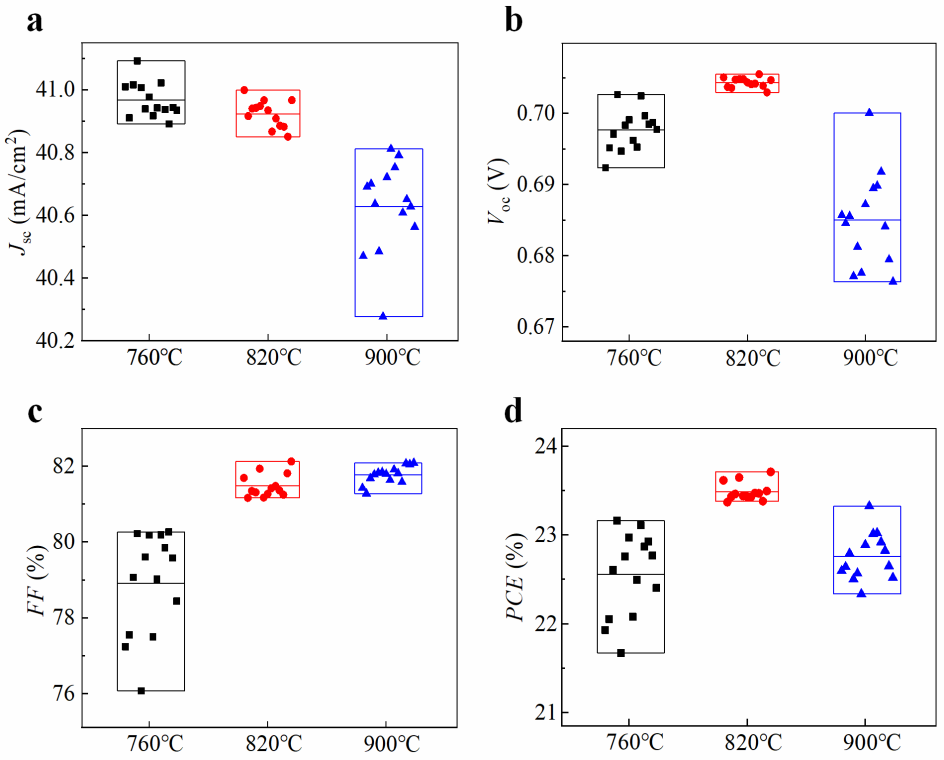

Figure 4.23 (a)-(d) Distributions of electrical parameters under the various T_a.

4.5.3 Loss Analysis

To clarify the recombination components, the distribution of current recombination at the respective maximum power point (MPP) conditions was simulated. The simulated *J-V* characteristic curves are presented in **Figure 4.24**a, where an additional resistance of 300 mΩ·cm^2 was introduced.

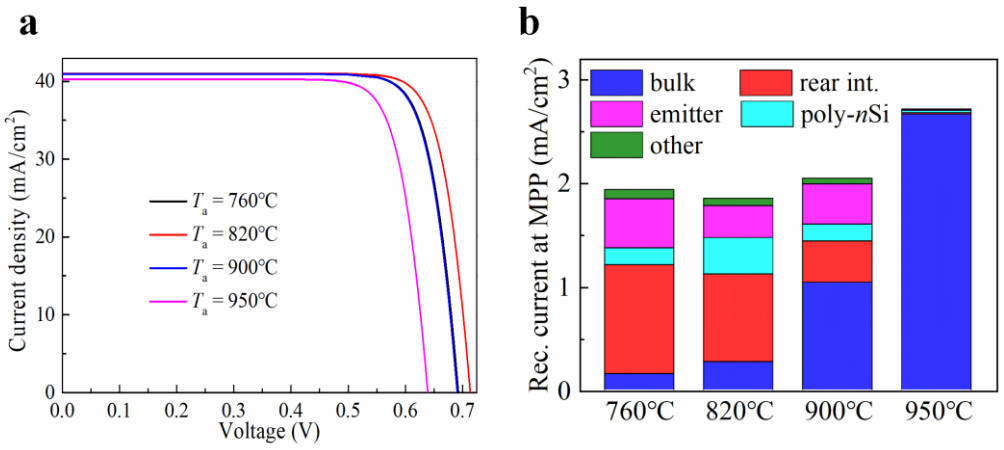

Figure 4.24 (a) Light *J-V* characteristic curves, and (b) distributions of recombination components at the respective MPP conditions under the different T_a.

Figure 4.24b clearly shows that as T_a increases from 760°C to 950°C, the recombination contribution from the rear interface (SiO_x/*n*-Si interface) decreases monotonically due to strengthened field intensity. However, due to increased Auger (higher in-diffusion depth) and/or SRH (higher pinhole density) recombination losses, the bulk recombination contribution increases significantly. Overall, the optimal T_a is determined to be 820°C by considering the interface and bulk recombination contributions.

4.5.4 Efficiency Prediction

To further investigate the impact of contact/passivation properties on cell efficiencies,

the predicted *PCE* values were demonstrated under various J_0 and ρ_c values, as shown in **Figure 4.25**. The experimental data points were also highlighted in the figure.

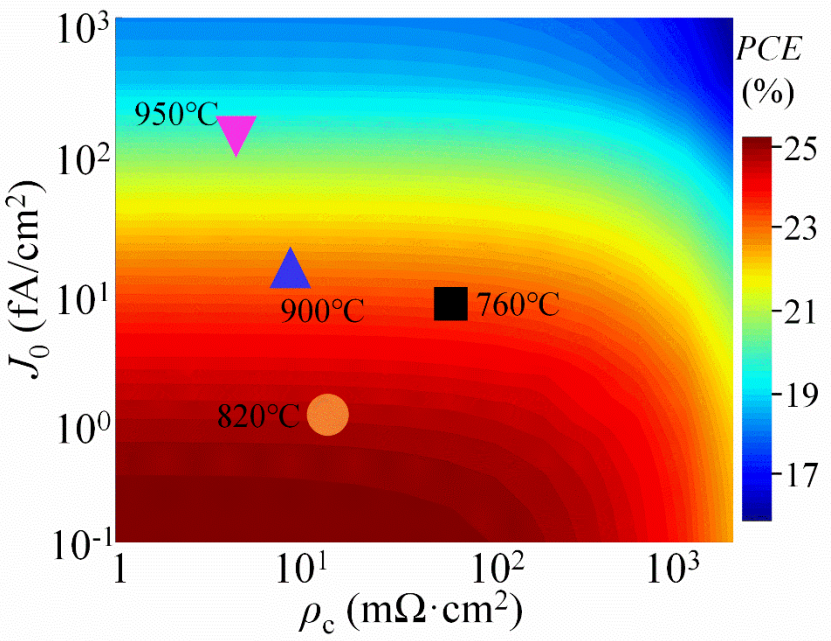

Figure 4.25 The predicted efficiencies under the various J_0 and ρ_c, where the typical cases under the different temperature annealing treatment extracted from Figure 4.17 were marked in the figure.

The simulation results indicate that: 1) J_0 has a significant impact on *PCE* values when J_0 exceeds 1 fA/cm^2, while ρ_c has a significant impact when ρ_c exceeds 10 mΩ·cm^2; 2) the experimental data points align with the simulated efficiency variations; 3) despite considering the best passivation (J_0 < 0.1 fA/cm^2) and contact (ρ_c < 1 mΩ·cm^2) properties, the simulated efficiencies are limited to about 25%, suggesting that the efficiencies of this type of TOPCon SCs are not restricted by the rear-sided poly-Si/SiO$_x$/*n*-Si contacts.

To assess the potential efficiency of this type of TOPCon solar cells, various strategies were proposed to further enhance the device efficiencies, as indicated in **Figure 4.26**. Specifically, under the optimal experimental parameters, the primary efficiency reached 24.2%. This was achieved with a J_0 value of 2.1 fA/cm^2 and a ρ_c value of 15.4 mΩ·cm^2 when T_a = 820°C. The passivation and contact of TOPCon structure can be further

improved by improving the quality of silicon oxide and polycrystalline silicon combined with annealing process. By improving the passivation and contact performance to a J_0 value of 0.1 fA/cm^2 and a ρ_c value of 1 mΩ·cm^2, a higher efficiency of 25.1% can be attained. Furthermore, by optimizing the doping profiles of the front emitters, as depicted in **Figure 4.27**, the efficiency of these TOPCon solar cells can be improved to 25.6%. Resistance loss can be further reduced by optimizing the electrode materials and design on the front and back sides, which can predict an efficiency of over 26%. Lastly, by adding a 120 nm-thick MgF_x antireflection layer on the front surface of the device to reduce the overall reflectivity, and by reducing parasitic absorption in the infrared band through C and N doped polycrystalline silicon, the current density of the device can be increased to 42.8 mA/cm^2. Through these optical strategies, the efficiency of the TOPCon solar cells can be improved to 27.2% (as indicated in **Figure 4.26**). This work outlines a technical roadmap for achieving efficiencies greater than 27% in TOPCon solar cells.[139] Furthermore, there have been reports of TOPCon solar cells with efficiencies exceeding 26%, indicating that achieving over 27% efficiency is also within reach.

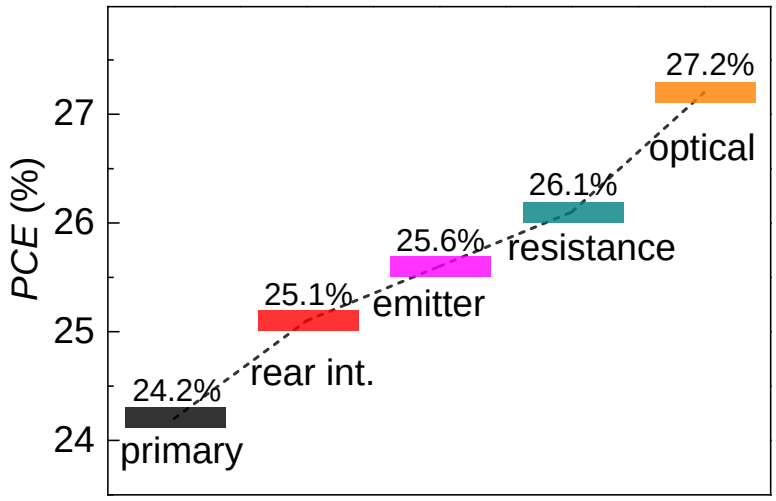

Figure 4.26 Roadmap of the efficiency improvement of TOPCon SCs.

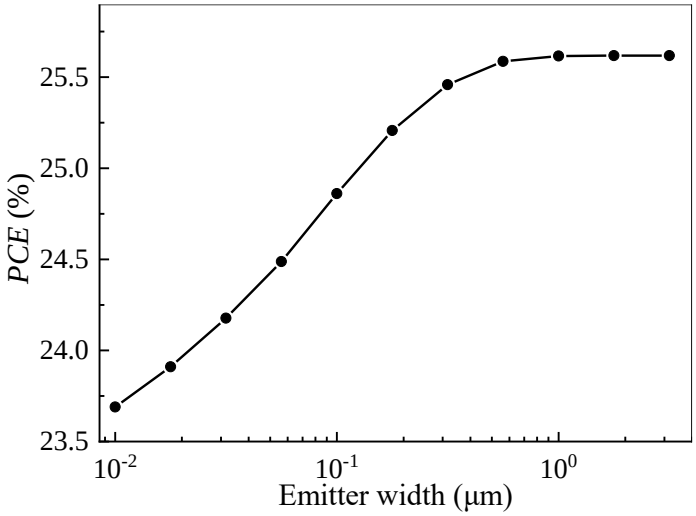

Figure 4.27 *PCE* values under the various emitter widths.

Moreover, numerical simulations were conducted to obtain the *J-V* characteristic curves corresponding to the optimized processes, with the results presented in **Figure 4.28**. In summary, this study provides a comprehensive technical plan for achieving efficiencies above 27% in TOPCon solar cells.

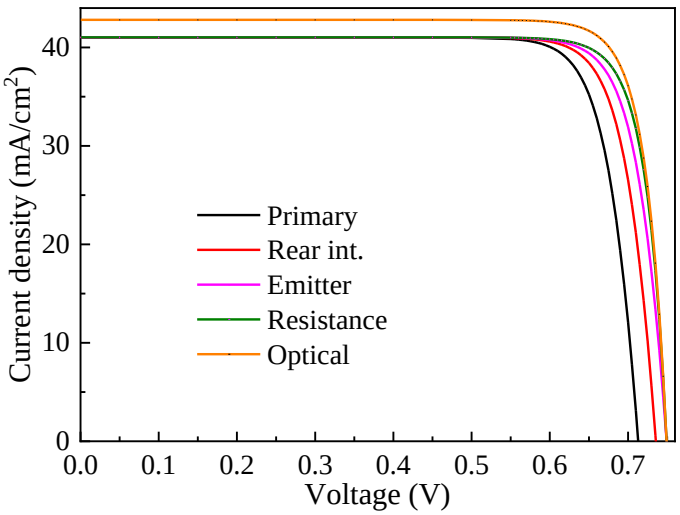

Figure 4.28 Simulated light *J–V* curves for the different *PCE* optimization process.

4.6 Conclusion

Elaborate simulations and experiments were conducted to uncover the underlying physical mechanism of the poly-Si/SiO_x/c-Si contact. TEM measurements revealed the presence of local SiO_x fractures with pinholes, and the density of these pinholes was determined through c-AFM measurements. The pinhole formation process was investigated by examining the film dynamics under different annealing conditions. It suggests that stress induced by the mismatch of coefficients of due to thermal expansion would be responsible for SiO_x film fracture. Numerical simulations were employed to review the charge-carrier transport mechanism in the poly-Si/SiO_x/c-Si contact. It indicates that both tunneling and pinhole transport mechanisms are present and interact with each other. The dominant mechanism depends on factors such as pinhole density/size and SiO_x thickness under specific fabrication conditions. The passivation and contact performance of this contact were experimentally studied by assessing the iV_{oc} and contact conductivity measurements. A fundamental physical model was established, considering both passivation and contact behavior simultaneously, to evaluate the potential efficiencies of the devices. Furthermore, proof-of-concept devices with complete cell structures exhibited high efficiencies, with an average value surpassing 23.5% at T_a = 820℃. This suggests that the combined effect of passivation and contact properties significantly contributes to the high performance of the devices. Detailed current-recombination analysis and predictions were performed, offering a specific roadmap for enhancing device efficiency.

Chapter 5 Perovskite Solar Cells

5.1 Synopsis

Similar to crystalline silicon solar cells, perovskite solar cells (PSCs) also require cost reduction and efficiency improvement to enhance their competitiveness and practical application.[167] PSCs offer unique advantages in terms of bandgap and thickness regulation of the perovskite layer, leading to various derivative applications such as semi-transparent devices,[168,169] flexible devices,[170,171] and top-side SCs for tandem devices[172-175]. Whether it is for standalone PSCs or these derivative applications, achieving high device efficiencies is crucial for improving competitiveness. Currently, traditional approaches to enhance PSC efficiency involve passivating interface defects, modifying functional layers, and improving the quality of perovskite films. While these strategies have successfully pushed the efficiencies of PSCs beyond 25%, further improvements are becoming increasingly challenging.

One effective way to enhance the optical response and increase the short-circuit current density (J_{sc}) in PSCs is through optical management techniques, similar to those employed in crystalline silicon solar cells. Additionally, advanced optical structures such as interdigitated back contact (IBC) design hold promise for improving the optical performance of PSCs. With IBC PSCs, the parasitic absorption resulting from carrier selective transport layers and transparent electrodes in the conventional sandwich design can be mitigated. The absence of a front-side electrode allows for greater material selectivity. Furthermore, the IBC design facilitates the investigation of photon recycling (PR)[176] in perovskite-based devices and enables *in-situ* or *in-operando* characterization of perovskite films.[177] Currently, research on IBC PSCs is in its early stages, and the development of theoretical models is necessary to understand the carrier transport mechanisms and predict device efficiency.

This chapter introduces two methods to promote the efficiencies of PSCs, *i.e.*, optical

and IBC structure designs. For the optical design, the Gaussian structured gradient-index optical structures were proposed. For the IBC design, the electrical and optical properties were systematic investigated.

5.2 Gaussian Structured Gradient-Index Optical Design

This section introduces an advanced gradient-index optical design for perovskite solar cells (PSCs) by texturing the front-sided glass substrate using Gaussian-shaped structures. The optimization of the structure, optical properties, and light-trapping mechanism are presented.

5.2.1 Simulation Details

The numerical simulations were conducted using the finite-element method based on the platform of COMSOL Multiphysics, which solves Maxwell's equations in the frequency domain to obtain the spatial electromagnetic distributions. Three-dimensional (3D) simulations were performed with symmetrical/anti-symmetric periodic boundary conditions, utilizing perfectly electric/magnetic conductors. The wavelength range of interest was set from 300 nm to 800 nm. The refractive indexes of various materials used in the simulations, including glass, fluorine-doped tin oxide (FTO), titanium oxide (TiO_2), perovskite, Spiro-OMeTAD (Spiro), and gold (Au), were extracted from the reference,[178] which were also plotted in **Figure 5.1**.

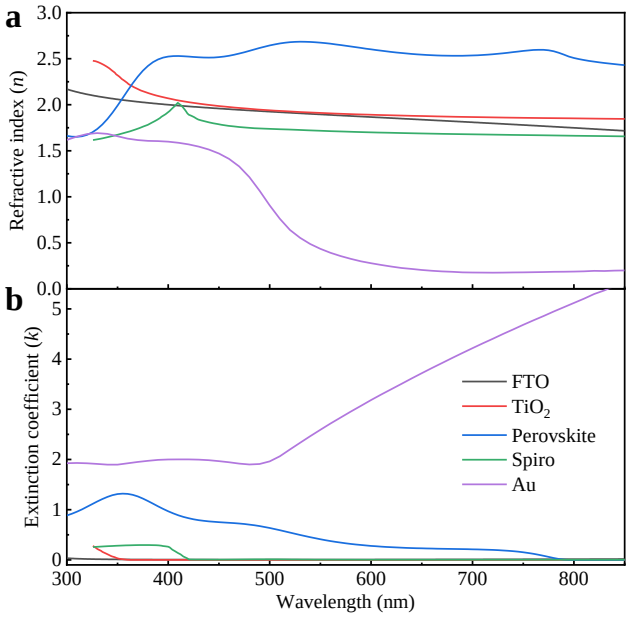

Figure 5.1 (a) Refractive index (n) and (b) extinction coefficient (k) of the related materials used in this simulation.

Figure 5.2a illustrates the schematic used for the simulations, where the front-side surface was textured with a Gaussian-shaped optical design. The thickness of the FTO/TiO_2/perovskite/Spiro-OMeTAD layers was maintained at 150/50/350/250 nm, as referenced.[179] The halide perovskite ($CH_3NH_3PbX_3$) with a bandgap of approximately 1.55 eV was utilized, corresponding to an absorption cutoff at 800 nm.

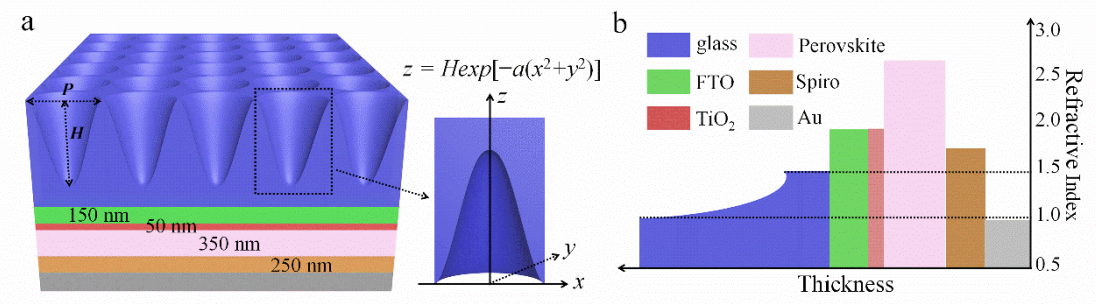

Figure 5.2 (a) Schematic diagram of simulation devices. (b) Distributions of the effective refractive indexes at wavelength of 500 nm.

The Gaussian-type optical structure used in this simulation can be described by the following equation:[74]

$$z = Hexp[-a(x^2 + y^2)] \quad (5.1)$$

where H represents the height size, and a is the control factor of the Gaussian-shaped optical structures. The effective refractive index (n) can be calculated using the following equation:[74]

$$n(z) = n_{\text{glass}} - \left(n_{\text{glass}} - 1\right)\frac{\pi}{aP^2} In(\frac{H}{z}) \quad (5.2)$$

where n_{glass} is the refractive index of the glass substrate, and P is the *pitch* of the Gaussian-shaped optical design. **Figure 5.2**b illustrates the effective refractive index at λ = 500 nm, indicating a gradient-index within the glass film. Solving Maxwell's equations allows for accurate optical modeling without the need for approximations. In the case of the effective refractive index (n) calculation mentioned, it is an approximation used to demonstrate the trend of refractive index variation within the Gaussian-type structure. This simplified approach helps provide a general understanding of the optical behavior without the need for a detailed and computationally intensive calculation.

5.2.2 Structure Optimization and Spectra Response

Figure 5.3 presents the optimization of the photocurrent density (J_{ph}) for the Gaussian-type structures by investigating relevant parameters such as H and P. In the case without Gaussian-type structures (*i.e.*, H = 0), a relatively low J_{ph} value of 22.14 mA/cm^2 was observed. However, with the inclusion of Gaussian-type structures, a significant improvement in J_{ph} was observed, particularly for H values greater than 300 nm. Moreover, the figure reveals that J_{ph} initially increases with increasing H from 0 to 570 nm and then decreases with further increasing H from 570 to 1000 nm. The maximum J_{ph} value of 23.35 mA/cm^2 was obtained at H = 570 nm and P = 650 nm (indicated by the white star), representing a J_{ph} enhancement of over 1.2 mA/cm^2 through the Gaussian-type structure design.

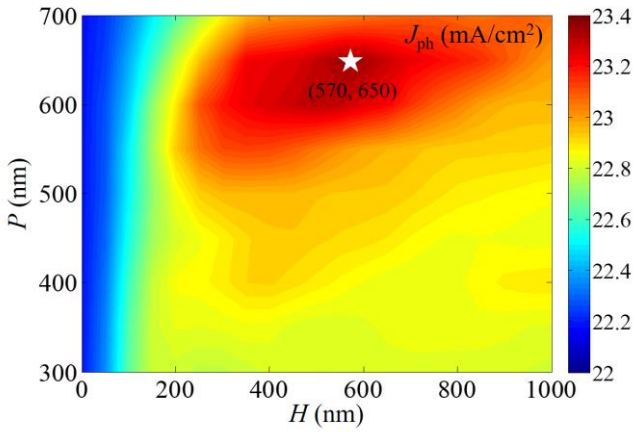

Figure 5.3 J_{ph} under the different H and P, where the maximum was marked by the white star (H = 570 nm & P = 650 nm).

Furthermore, **Figure 5.4**a provides a detailed analysis of the optical absorption from the perovskite layer (*Abs*) and the reflection loss from the front-side surface (*R*) for the flat and optimized Gaussian-type structures across the wavelength range of 300 nm to 800 nm. Additionally, the experimental *EQE* spectrum with the same structural configuration is included for comparison, which was extracted from reference.[12] For the flat cases, the simulated *Abs* (marked by the blue line) and the experimental *EQE* (marked by black circles) exhibit similar trends. However, the simulated *Abs* shows pronounced resonance behavior within the wavelength range of interest, which is expected since the simulated structure is an ideal flat structure that can induce Fabry-Perot (FP) resonance effects and lead to oscillatory behavior. In contrast, the experimental flat structure does not possess an ideal flat surface, thus lacking the observed oscillatory behavior. Consequently, the simulated J_{ph} and the experimental J_{sc} calculated by weighting the corresponding spectra under AM1.5G were 22.14 and 22.34 mA/cm^2, respectively.

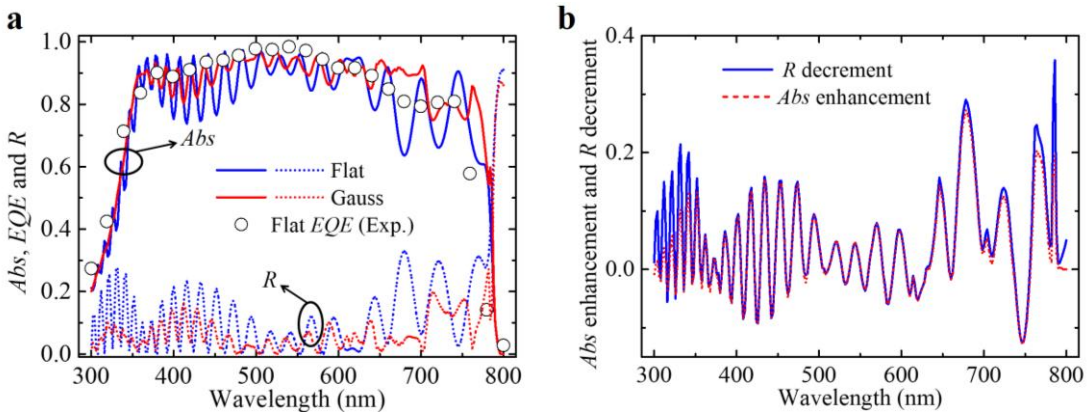

Figure 5.4 (a) Spectra of *R*, *EQE* and *Abs* of the relevant cases. The experimental *EQE* of the device with flat glass structure are included for comparison. (b) *R* decrement and *Abs* enhancement between the two cases. Here, the experimental *EQE* spectrum is extracted from reference.

It is worth noting that the experimental J_{sc} obtained from the *J-V* characteristics was 22.75 mA/cm^2,[12] slightly higher than the previously mentioned cases. The *Abs* spectrum of the simulated Gaussian-type structure (red line) is also presented in **Figure 5.4**, demonstrating higher values and smaller amplitudes compared to the flat case. To facilitate comparisons, **Figure 5.4**b displays the *Abs* enhancement and *R* decrement between the flat and Gaussian-type structure cases. The results reveal that: 1) the *Abs* enhancement is mostly positive across a wide range of wavelengths, indicating a broadband optical absorption response due to the design of the front-side Gaussian structure; 2) the *Abs* enhancement is slightly lower than the *R* decrement, suggesting the presence of strong parasitic absorption.

To further quantify the optical response, the current density distributions, including parasitic absorption, *R*, and *Abs*, are depicted as a histogram in **Figure 5.5**. The Gauss case exhibits slightly increased parasitic absorption losses in the related layers of FTO/TiO_2/Spiro/Au, with values ranging from 0.73/0.1/0.12/0.33 mA/cm^2 to 0.85/0.11/0.15/0.34 mA/cm^2. These improved parasitic absorption losses in the Gauss case are a result of the enhanced optical-path length. Importantly, the current density caused by front-side reflection loss is reduced to 2.55 mA/cm^2 for the Gauss case (compared to 3.93 mA/cm^2 for the flat case), leading to a 1.21 mA/cm^2 improvement

in J_{ph}, *i.e.*, from 22.14 mA/cm^2 (Flat) to 23.35 mA/cm^2 (Gauss).

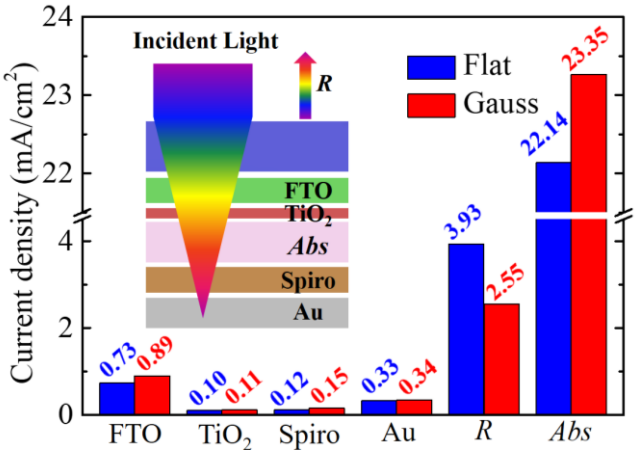

Figure 5.5 Distributions of perovskite absorption (*Abs*) and optical losses including the front-side reflection loss (*R*) and parasitic absorption in the related layers.

The control factor (*a*), which defines the Gaussian-type architecture, has a significant impact on the effective optical absorption. As shown in **Figure 5.6**, when the control factor, *a*, increases from 1 to $10\times4/P^2$, J_{ph} initially increases and then decreases, with the optimized J_{ph} occurring at $a = 20/P^2$. For comparison, the corresponding J_{ph} values of 22.14 mA/cm^2 and 22.94 mA/cm^2 are marked in the figure for the flat and nanohole array counterparts, respectively. It is evident that the Gaussian-type structure consistently achieves a high J_{ph} exceeding 23 mA/cm^2 regardless of the value of *a*, surpassing the flat and nanohole counterparts. In summary, the introduction of the Gaussian-type architecture could promote the optical response with improved photocurrent value compared with the flat counterpart.

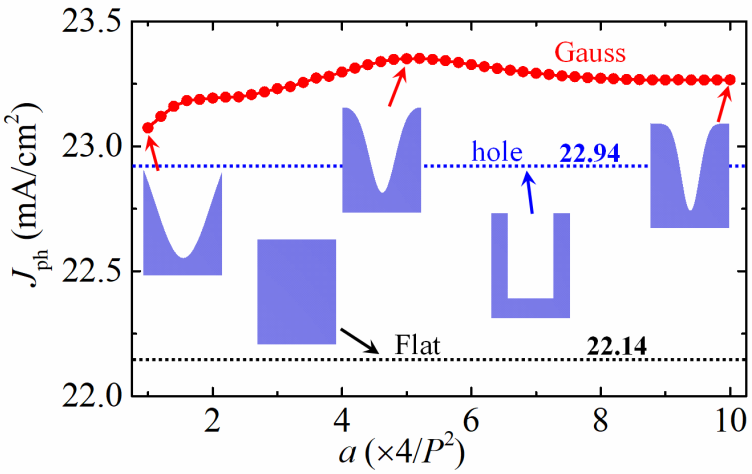

Figure 5.6 J_{ph} under the different a, where the normal cases with flat and hole (H = 570, P = 650 nm) counterparts were also marked in figure. The insets show the corresponding index structures, namely the flat, hollow and the various Gaussian-type designs.

5.2.3 Light-Harvesting Mechanism

To gain further insight into the optical management mechanism of the Gaussian-type design, **Figure 5.7** presents the electric field distributions at wavelengths of 418, 646, and 764 nm. The profiles for the Gauss structure at the middle and border positions of a unit are considered, along with the flat counterpart having the same structure configuration for comparison.

In the case of the flat structure, typical Fabry-Perot (FP) resonance modes can be observed at the three wavelengths, resulting in equal electric field intensity at corresponding depths. However, the presence of the Gaussian-type structure leads to the formation of numerous hotspots throughout the region, significantly enhancing the spatial electric field intensity. The red region highlights the electric field distributions in the perovskite layer. At 418 nm, the electric field distributions in the perovskite layer mainly concentrate on the top region due to the high extinction coefficient inherent to the perovskite material. This results in strong optical absorption and a shortened penetration depth. Notably, the electric field intensity is particularly enhanced,

especially at the double side positions of the Gauss border case, where two hotspots are present. For the latter two wavelengths, the electric field distributions spread across the entire perovskite layer, exhibiting the spatial electric field for the Gauss cases. The improved optical response can be attributed to the presence of numerous high-order resonance modes induced by the Gaussian-type design, which effectively increases the effective optical path.

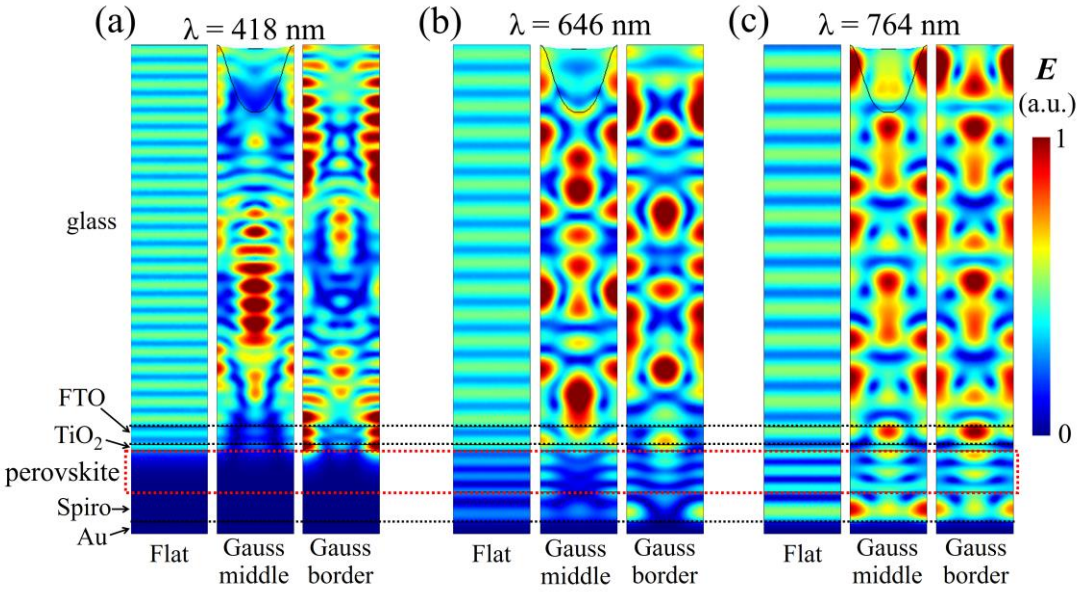

Figure 5.7 (a)-(c) Electric-field distributions under three representative wavelengths of 418 nm, 646 nm and 764 nm.

5.2.4 Perovskite Thickness and Incident Angle

The aforementioned results are based on a fixed perovskite thickness of 350 nm. Investigating the optical response of these PSCs with varying perovskite thickness is of significant importance. **Figure 5.8** displays the J_{ph} of the two structures considered, as well as the J_{ph} enhancement with increasing perovskite thickness. For both cases, J_{ph} exhibits rapid improvement as the perovskite thickness increases from 50 nm to 350 nm, followed by a relatively stable trend from 350 nm to 800 nm. The graph clearly illustrates a tendency of J_{ph} to increase and then decrease with increasing perovskite

thickness from 50 nm to 800 nm. In the case of 50 nm-thick PSCs, the perovskite thickness is insufficient to adequately absorb the incident light, resulting in low J_{ph} and a low J_{ph} enhancement. However, increasing the perovskite thickness from 100 nm to 800 nm effectively promotes optical absorption in the perovskite film for both structures, resulting in high J_{ph} values but a relatively low J_{ph} enhancement. Notably, the best J_{ph} enhancement of over 2 mA/cm^2 is achieved for the 100 nm-thick perovskite case. Consequently, the Gaussian-type structure design can improve the J_{ph} of these PSCs, especially for thin PSCs.

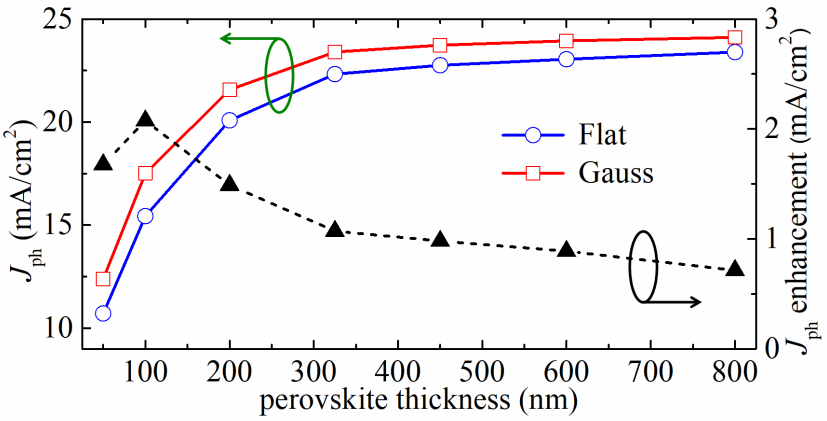

Figure 5.8 J_{ph} and J_{ph} enhancement under the different perovskite thicknesses.

The photocurrent properties of these PSCs were further investigated under different incident angles, as shown in **Figure 5.9**. The simulation diagram is included in the figure for reference. In comparison to the flat structure cases, the Gaussian-type structures exhibit high J_{ph} values across the entire range of considered angles ($-85° < \theta < 85°$). **Figure 5.9** also includes a black dot line representing the ratio of J_{ph} enhancement between flat and Gaussian-type structures for comparison. As the incident angle θ increases from 0° to 85°, the ratio of J_{ph} enhancement gradually increases from 1.05 to 1.27. This indicates that the introduction of Gaussian-type structures can enhance the optical response compared to the flat case, particularly for larger incident angles. It should be noted that although the best J_{ph} value achieved through this simulation is not significantly higher than the highest value obtained with a normal flat

structure, the introduction of the Gaussian-type design provides a novel approach to achieve a wideband, omnidirectional antireflective profile, thereby improving the overall optical response.

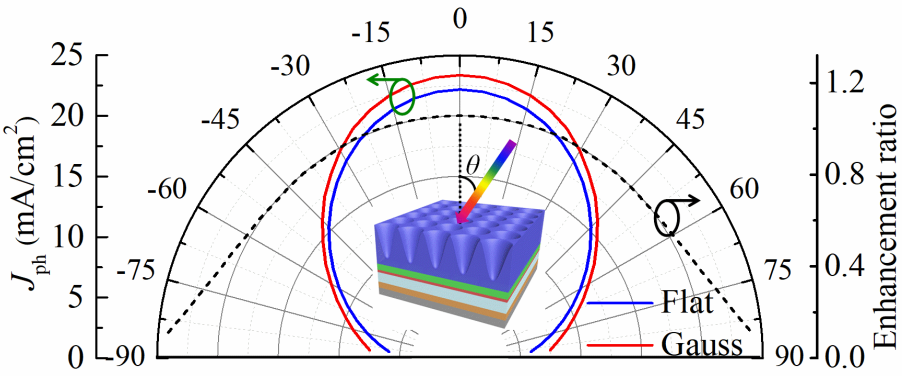

Figure 5.9 Angle-dependent J_{ph} and J_{ph} enhancement proportion. The inset is the simulation diagram. Here, *P* and *H* for the Gaussian-type structures were fixed at 650 nm and 570 nm, respectively.

5.2.5 Conclusion

A Gaussian-type optical structure was proposed, and its optical properties were numerically investigated. Through this advanced design, a predicted best photocurrent density of 23.35 mA/cm^2 was achieved with a pitch of 650 nm and a height of 570 nm. This value is 1.21 mA/cm^2 higher than that of the normal flat structure, which has a current value of 22.14 mA/cm^2. The optical properties of these Gaussian-type structures can be effectively improved by reducing the reflection loss, which is reduced to 2.55 mA/cm^2 compared to 3.93 mA/cm^2 for the flat structures. The improved optical management in the perovskite layer results in broadband optical enhancement across most wavelengths from 300 nm to 800 nm. The optical management mechanism was further clarified by analyzing the electric-field distributions. Furthermore, the PSCs with Gaussian-type structures exhibit outstanding optical properties regardless of the perovskite thickness. Compared to flat structures, Gaussian surface-patterned PSCs also demonstrate higher tolerance to incident angles, making them suitable for solar

cells that require effective antireflection over a wide range of angles.

5.3 IBC Perovskite Solar Cells

This section presents a comprehensive photoelectrical model for interdigitated back contact (IBC) perovskite solar cells (PSCs). The model incorporates numerical simulations by combining traditional drift-diffusion equations to determine charge transport behavior and ion migration equations to account for ion transport behavior with the photon recycling effect. By examining the relevant electrical parameters and analyzing the charge generation, transport, recombination, and collection processes, the device physics of IBC PSCs are thoroughly explained.

5.3.1 Simulation Details

The IBC devices with a quasi-interdigitated back contact (QIBC) configuration are depicted in **Figure 5.10**. These devices are considered a flexible approach due to their simplified manufacturing process and relatively long charge transport length, as confirmed by Deschler *et al*.[88] In the QIBC devices, carriers are required to transport in both lateral and vertical directions within the PSCs before being collected by the corresponding contacts or electrodes. The simulated devices with QIBC structures are modeled, where the electron transport layer (ETL) and hole transport layer (HTL) consist of a SnO_2 layer and a NiO_x layer, respectively, with thicknesses of 100 nm and 50 nm. An Al_2O_3 insulating layer, approximately 100 nm thick, is inserted between the two contacts to separate the HTL and ETL. A fluorine-doped stannic oxide (FTO) film with a thickness of 500 nm serves as the negative contact, while a nickel metal (Ni) film with a thickness of 50 nm acts as the positive contact. A polymethyl methacrylate (PMMA) film is chosen as the front-sided anti-reflective coating (ARC). Additionally, the width of the HTL (W_{HTL}) and the *pitch* of the devices are maintained at 1 μm and 2 μm, respectively.

For the optical simulations, the finite element method (FEM) is employed. The optical parameters, including refractive index, used for these simulations are extracted from

reference.[178,180,181] Regarding the electrical simulations, the corresponding electrical parameters are tabulated in **Table 5.1**.

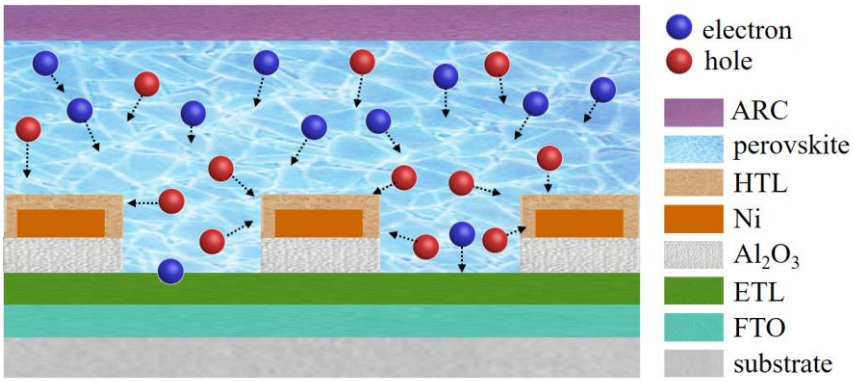

Figure 5.10 Simulated devices of QIBC PSCs.

Table 5.1 Electrical parameters used for simulation.

Material parameters	ETL	Perovskite	HTL
Thickness, nm	100	400-600	50
Electron affinity, χ (eV)	4.23	3.93	1.7
Bandgap energy, E_g (eV)	3.7	1.55	3.6
Relative dielectric permittivity, ε	9	6.5	12
Effective conduction band density, N_c (cm^{-3})	4.36×10^{18}	2.8×10^{18}	9.15×10^{17}
Effective valence band density, N_v (cm^{-3})	2.52×10^{19}	1.8×10^{19}	4.54×10^{18}
Donor doping concentration, N_d (cm^{-3})	1×10^{17}	/	/
Acceptor doping concentration, N_a (cm^{-3})	/	1×10^{13}	2.66×10^{17}
Mobility of electron/hole, μ_n/μ_p (cm^2/Vs)	$1.9\times10^{-3}/1.9\times10^{-3}$	12.5/7.5	0.01/0.01
SRH life time, τ_n/τ_p (s)	0.083/0.083	$2.73\times10^{-6}/2.73\times10^{-6}$	$1\times10^{-6}/1\times10^{-6}$
Radiative recombination coefficient, B_{rad} (cm^3s^{-1})	/	3.27×10^{-11}	/
Auger recombination coefficient, A_n/A_p (cm^6s^{-1})	/	0.88×10^{-29}	/

5.3.2 Optical Response

Based on the optical simulations, the profile of the charge-carrier generation ratio in the perovskite layer is demonstrated in **Figure 5.11**a. In comparison to the normal flat structure, which exhibits uniform carrier generation, this type of IBC device exhibits position-dependent carrier generation. Furthermore, **Figure 5.11**b and **5.11**c depict the position- and depth-dependent carrier generation ratios, respectively.

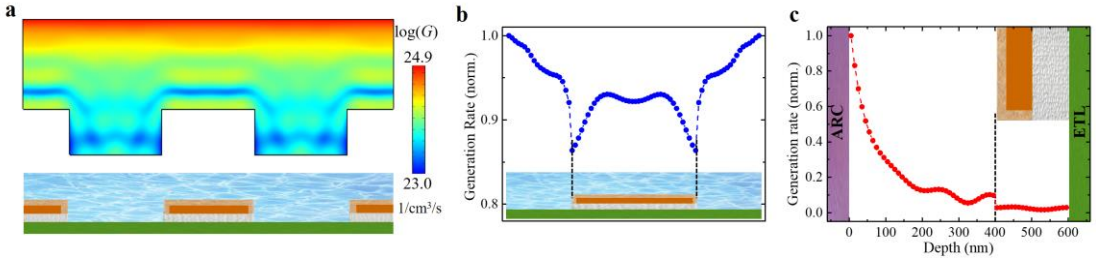

Figure 5.11 (a) Profile of charge-carrier generation ratio in perovskite film. (b) Position- and (c) depth-dependent carrier generation ratios.

From **Figure 5.11**b, it can be found that the average optical absorption efficiencies show the highest values at the middle position of HTL and the lowest values at ETL/HTL contact. The carrier generation rate as a function of depth demonstrated in **Figure 5.11**c suggests a depth-decreasing trend, revealing that carrier generation is enriched in the front-side of perovskite film. The carrier generation profile observed in these results aligns with the findings proposed by Koster *et al.*,[182] confirming the reliability of my results.

Figure 5.12 displays the wavelength-dependent spectra, including the reflection of the entire device (*Ref*), optical absorption in the perovskite film (*Abs*), and parasitic absorption loss from the functional layers (*Para Abs*). It is evident that the optical performance between 300 nm and 600 nm is improved due to the presence of the IBC design. The simulation results indicate that this type of QIBC PSCs achieve a predicted J_{ph} of 24.26 mA/cm^2, with 2.50 mA/cm^2 contributed by reflection and 0.73 mA/cm^2

attributed to parasitic absorption loss. **Figure 5.13** provides detailed plots of the parasitic absorption spectra from the different components, indicating that the primary source of parasitic absorption losses is the Ni and FTO layers.

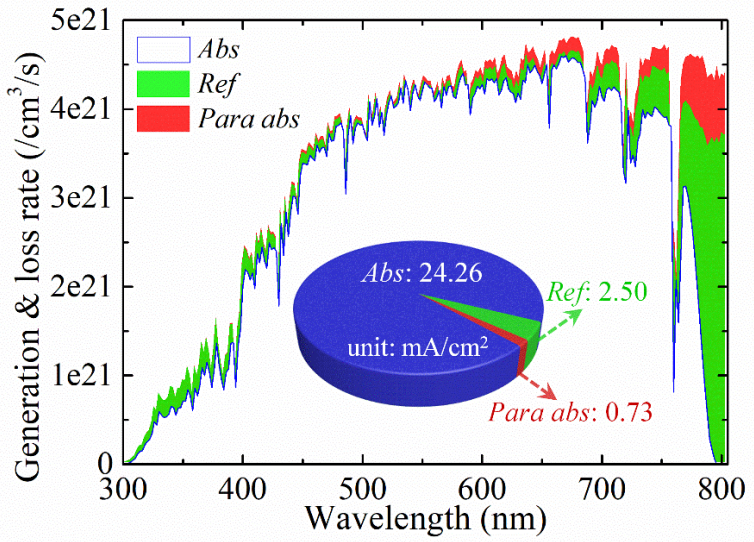

Figure 5.12 *Abs*, *Ref*, and *Para abs* spectra and the corresponding current distributions for the device with an average perovskite thickness of 500 nm.

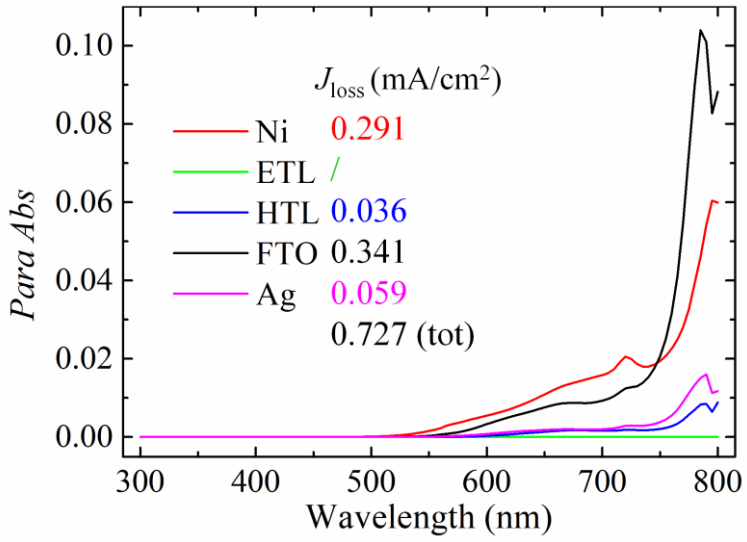

Figure 5.13 Parasitic absorption spectra of this kind of QIBC PSCs.

For the purpose of comparison, **Figure 5.14** demonstrates normal sandwich devices with identical photoelectrical parameters. These devices exhibit a relatively low J_{ph}

value of only 22.38 mA/cm^2, a higher current density due to reflection loss (2.87 mA/cm^2), and a significantly higher current density resulting from parasitic absorption (2.37 mA/cm^2). The improved parasitic absorption losses in the QIBC design primarily arise from the absorption of the Ni, ETL, and FTO layers. Consequently, it can be concluded that implementing the QIBC design in PSC devices effectively enhances the optical performance by reducing optical reflection losses and lowering parasitic absorption losses from the functional layers.

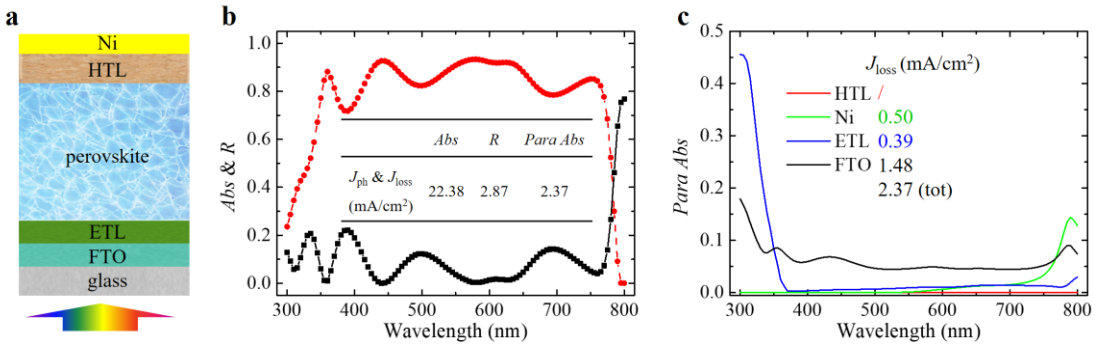

Figure 5.14 (a) Sketch map of the normal sandwich PSCs. (b) *Abs* and *Ref* spectra and the corresponding current distributions. (c) Parasitic absorption spectra of the normal sandwich PSCs.

It is worth noting that in Koster's experiment, the effective thicknesses of the perovskite layer and Anti-Reflection Coating (ARC) are 300 nm and 50 nm, respectively. Therefore, it is necessary to investigate the impact of these thicknesses on the optical performance in order to achieve the optimal optical response. **Figure 5.15** predicts a relatively poor J_{ph} value of 21.37 mA/cm^2 for the case of a 300 nm-thick perovskite layer due to enhanced reflection and transmission losses. **Figure 5.16** shows that as the ARC thickness increases from 0 to 150 nm, J_{ph} initially increases and then decreases, reaching its highest value at an ARC thickness of 80 nm. These results suggest that, for QIBC PSCs, a relatively thick perovskite film and a suitable ARC thickness should be adopted to ensure high optical performance.

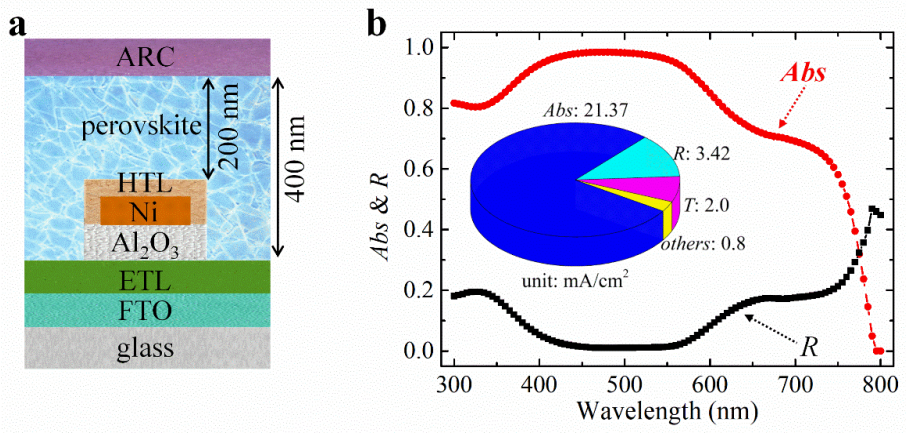

Figure 5.15 (a) Sketch map of QIBC PSCs and (b) *Abs* and *Ref* spectra and the corresponding current distributions for the device with an average perovskite thickness of 300 nm.

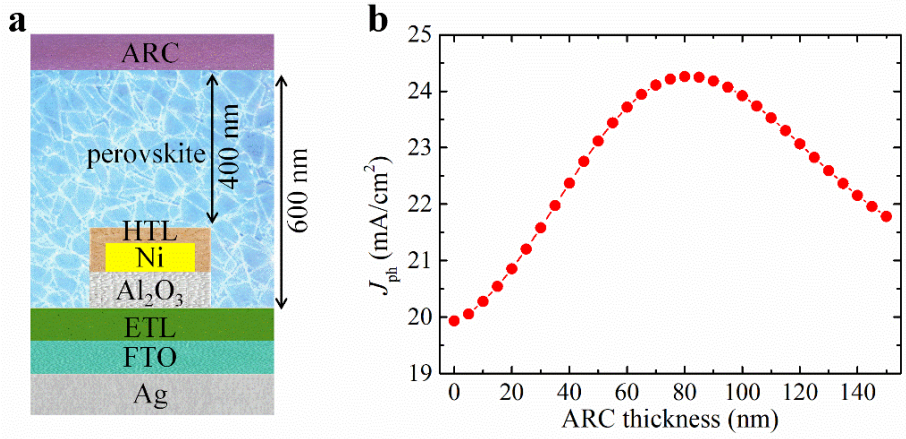

Figure 5.16 (a) Sketch map of QIBC PSCs with an effective perovskite thickness of 500 nm. (b) J_{ph} under the different ARC thicknesses.

5.3.3 Dependence of Electrical Parameters

By implementing the detailed photoelectrical model, the performance of PSCs was thoroughly evaluated. **Figures 5.17-5.21** illustrate the relationship between electrical parameters (defect density, surface recombination velocity, and mobility) and the device performance of QIBC PSCs. For comparison, devices with traditional sandwich structures were also demonstrated.

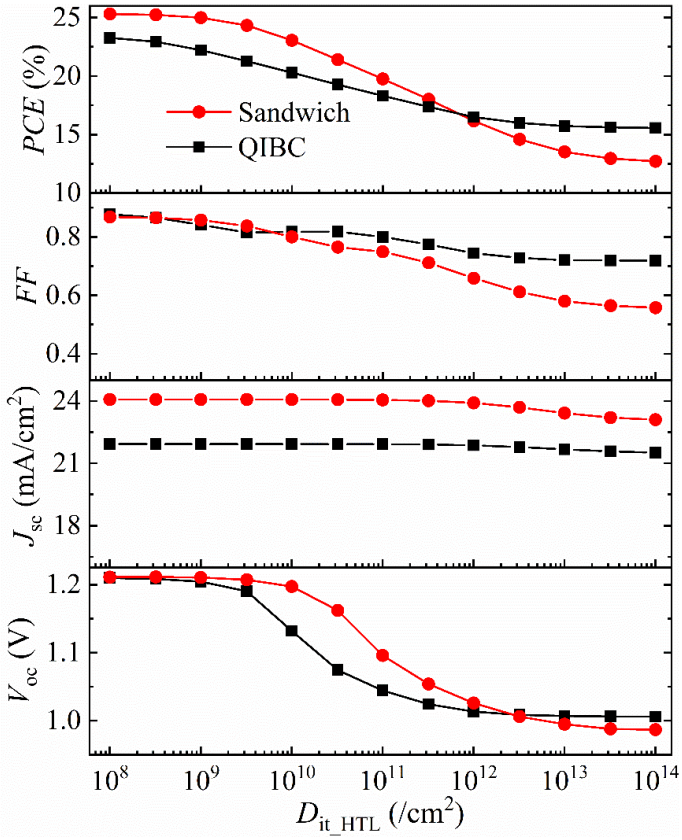

Figure 5.17 Effects of D_{it_HTL} on device electrical parameters under D_{it_ETL} = 10^8 cm^{-2} & S_{top} = 1 cm/s.

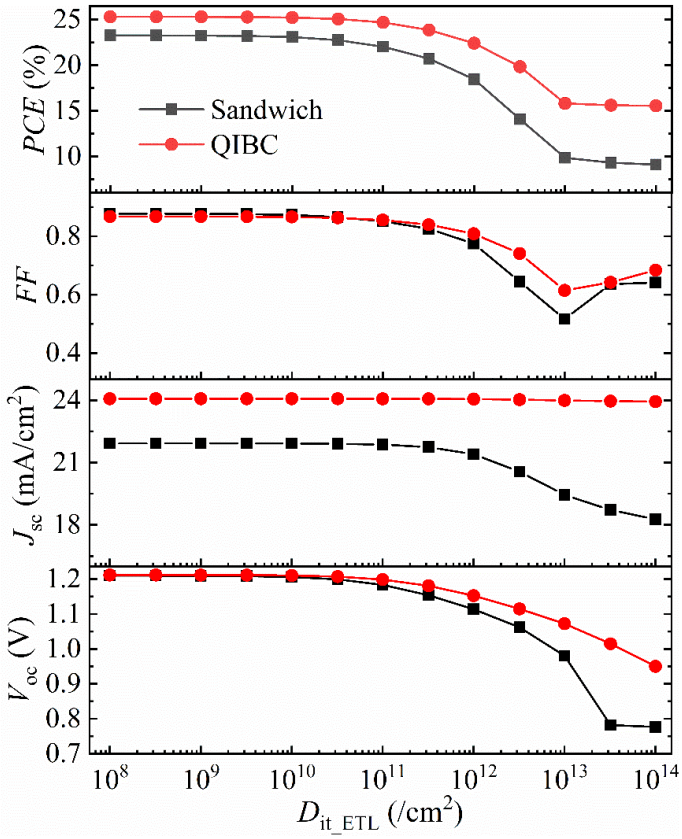

Figure 5.18 Effects of D_{it_ETL} on device electrical parameters under D_{it_HTL} = 10^8 cm^{-2} & S_{top} = 1 cm/s.

Analyzing **Figures 5.17** and **5.18**, it is evident that the *PCE* values for both QIBC and sandwich cases exhibit a monotonous reduction trend as D_{it_HTL} increases from 10^8 cm^{-2} to 10^{14} cm^{-2}. However, the *PCE* values can be maintained effectively when D_{it_ETL} is less than 10^{11} cm^{-2}. Subsequently, they decline significantly when D_{it_ETL} exceeds 10^{11} cm^{-2}. Furthermore, as D_{it_HTL} increases from 10^8 cm^{-2} to 10^{14} cm^{-2}, defects in the HTL/perovskite interface affect the sandwich cases more severely, leading to more substantial degradation in *PCE*. This degradation may be attributed to the reduced collection area for QIBC cases. Conversely, defects in the ETL/perovskite interface have a greater impact on the QIBC cases when $D_{it\_ETL} > 10^{12}$ cm^{-2}. In these cases, the enriched photogenerated carriers on the front-side of the perovskite layer (ETL side) cannot be effectively separated by the ETL contact in the sandwich structure. Consequently, an increased recombination loss occurs due to relatively higher recombination velocity, resulting in more significant degradation in *PCE* for the QIBC

cases. Overall, these findings emphasize the importance of defect density and interface engineering in achieving efficient perovskite solar cells.

The effects of perovskite film properties, such as N_t (trap density) and μ_n (electron mobility), on the device electrical parameters were also investigated, as depicted in **Figures 5.19-5.20**. The simulation results indicate the following: 1) QIBC PSCs exhibit higher *PCE* values compared to sandwich structures when $N_t < 10^{14}$ cm^{-3} or $\mu_n > 0.3$ cm^2/Vs; 2) QIBC cases have lower tolerance to N_t and μ_n compared to sandwich cases due to the relatively long carrier transport length in the perovskite layer of QIBC PSCs.

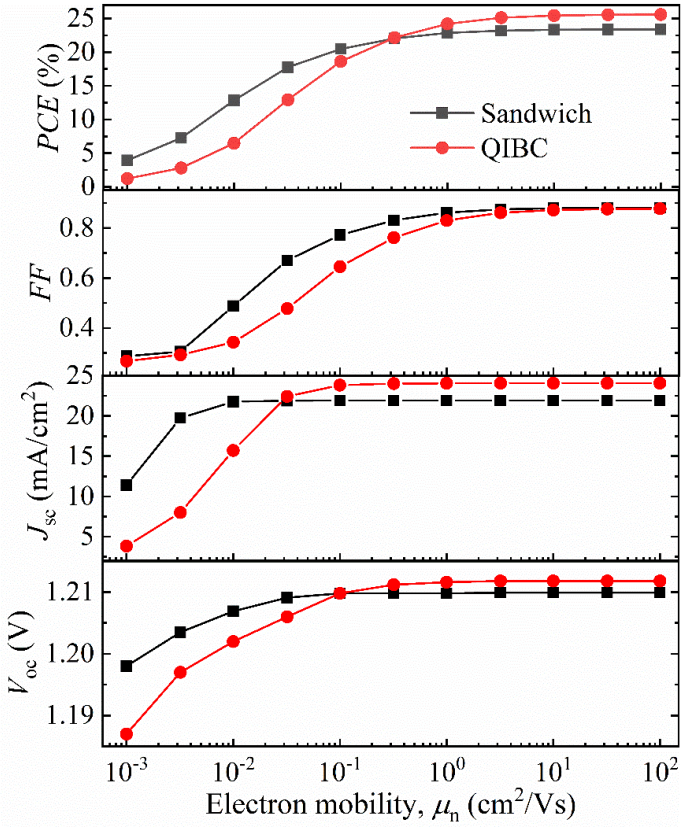

Figure 5.19 Effects of N_t on device electrical parameters under no interface defect case.

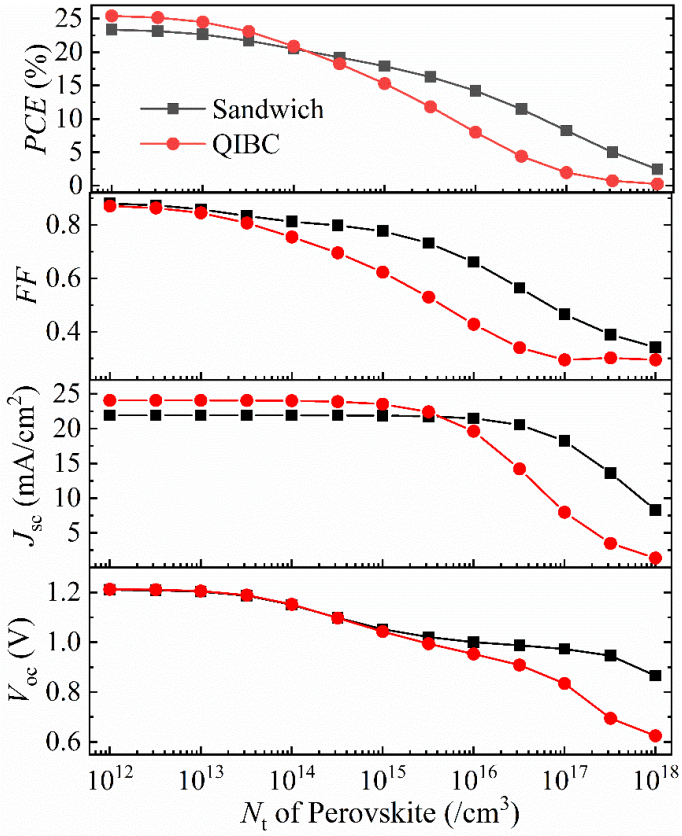

Figure 5.20 Effects of μ_n on device electrical parameters (hole mobility, $\mu_p = \mu_n/2$).

Additionally, the impact of front-side passivation quality (S_{top}) on device performance was evaluated in **Figure 5.21**. It is evident that increasing S_{top} from 1 cm/s to 10^4 cm/s results in a decrease in all electrical parameters, including *PCE*, *FF*, J_{sc}, and V_{oc}. This highlights the significance of front-side passivation in achieving desirable device performance. In summary, QIBC PSCs can achieve higher *PCE* values compared to traditional sandwich structures if electrical parameters such as N_t, μ_n, D_{it_HTL}, S_{top} and D_{it_ETL} are well-controlled. Furthermore, QIBC PSCs show the potential to achieve efficiencies beyond 25%, surpassing the efficiency of sandwich structures at 22.77%.[90] This indicates a promising future for QIBC PSCs in terms of efficiency.

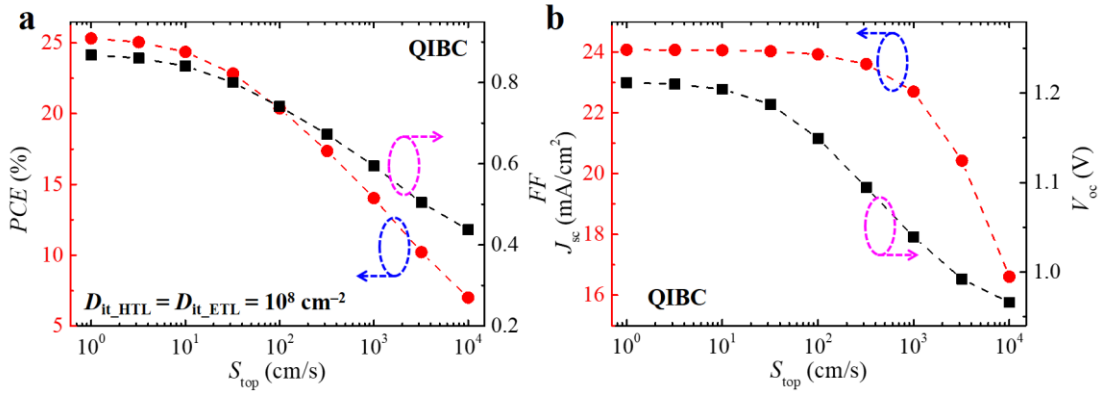

Figure 5.21 (a) *PCE* and *FF*, (b) J_{sc} and V_{oc} of this kind of QIBC PSCs under the different S_{top} at $D_{it\_HTL} = D_{it\_ETL} = 10^8$ cm^{-2}.

To further investigate the device electrical response of QIBC PSCs, **Figure 5.22** demonstrates V_{oc} as a function of light intensity. This parameter reflects trap-induced recombination within the perovskite layer and related interfaces.[66] For high-level passivation ($D_{it\_ETL} = D_{it\_HTL} = 10^8$ cm^{-2}), both sandwich and QIBC cases exhibit ideal factors with fitting slopes of 1.012/1.027 k_BT/q, respectively. In the case of moderate passivation ($D_{it\_ETL} = D_{it\_HTL} = 10^{10}$ cm^{-2}), the sandwich/QIBC PSCs display slopes of 1.32/1.26 k_BT/q, indicating suppressed trap-assisted recombination. These findings suggest that the QIBC structure can achieve high device performance when strict interface passivation is ensured.

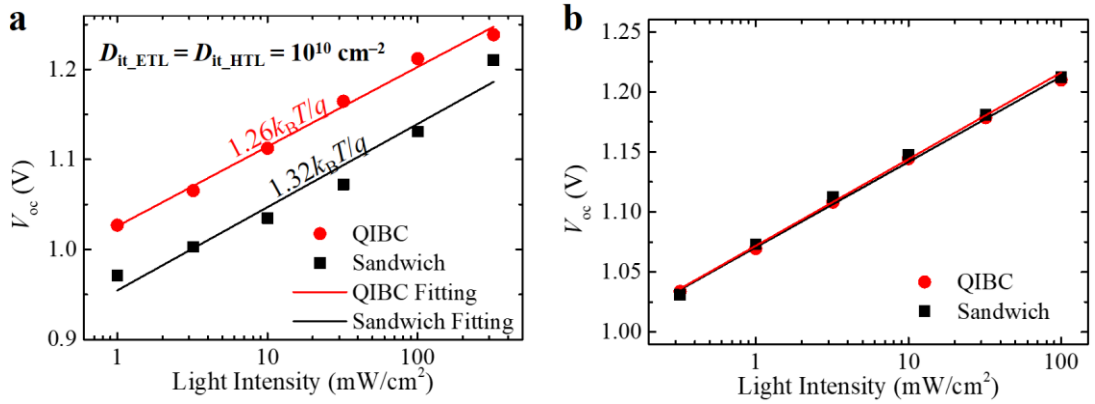

Figure 5.22 V_{oc} under the different light intensities for the two related cases under $D_{it\_HTL} = D_{it\_ETL}$ = (a) 10^8 cm^{-2}, and (b) 10^{10} cm^{-2}.

5.3.4 Carrier Recombination and Transport Mechanism

The dynamics of carrier transport in PSCs play a crucial role in determining charge carrier recombination and collection efficiency. It is important to analyze the recombination species involved. The histograms in **Figures 5.23**a and **5.23**b illustrate the recombination components of the two relevant cases at three representative points: open-circuit (OC), maximum power (MP), and short-circuit (SC).

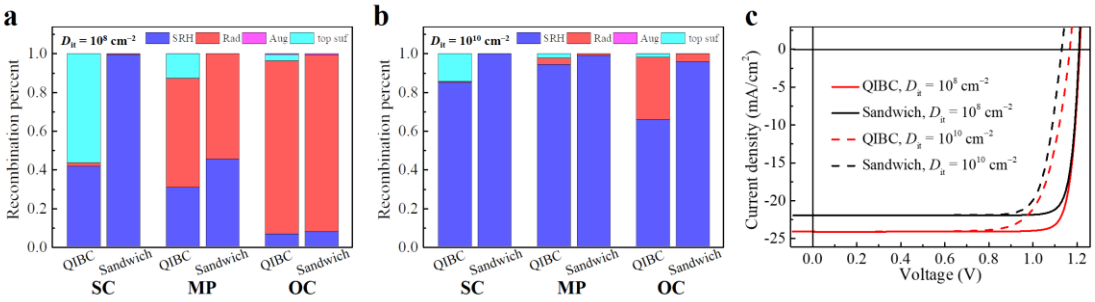

Figure 5.23 Distributions of recombination losses at three representative points for D_{it} equals to (a)/(b) 10^8/10^{10} cm^{-2}. (c) The corresponding *J-V* characteristic curves.

From **Figures 5.23**a and **5.23**b, it can be observed that Auger recombination losses can be neglected in all cases. For cases with high-quality passivation and a low D_{it} of 10^8 cm^{-2}, recombination losses in the studied PSCs are primarily caused by SRH recombination and surface recombination at the front-side during the SC case (**Figure 5.23**a). However, these losses are reduced at the MP or OC cases due to the increased contribution of radiative recombination. The recombination profiles for the three cases are depicted in **Figure 5.24**.

As D_{it} increases to 10^{10} cm^{-2}, it can be observed from **Figure 5.23**b that recombination losses from the radiative component are significantly reduced for all cases due to the increased dominance of SRH recombination. To further investigate the recombination mechanism, the light *J-V* curves of the two cases are shown in **Figure 5.23**c, indicating that increasing D_{it} (from 10^8 cm^{-2} to 10^{10} cm^{-2}) leads to degradation in device parameters such as V_{oc}, *FF*, and *PCE*.

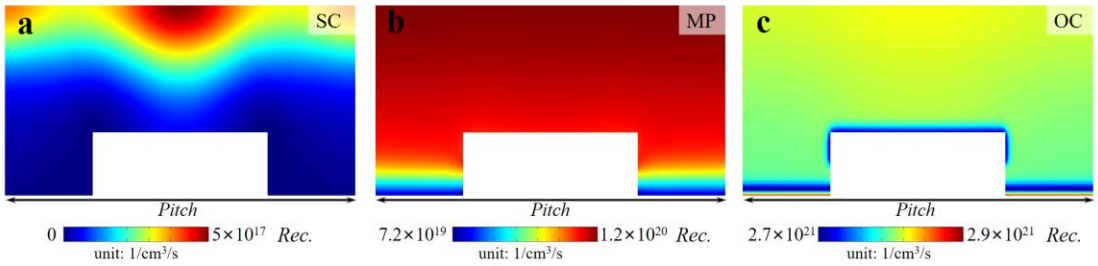

Figure 5.24 Spatial recombination profiles for QIBC PSCs under (a) SC, (b) MP and (c) OC cases.

To elucidate the charge carrier transport mechanism, the current densities of holes (J_p) and electrons (J_n) within the perovskite film are examined in **Figures 5.25**a and **5.25**b, respectively. Red arrows mark the consistent directions to illustrate the routes/channels of charge carriers. In **Figure 5.25**a, electrons transport almost vertically in the ETL region, while in the HTL region, electrons transport laterally and vertically simultaneously. Conversely, holes exhibit the inverse transport behavior, as shown in **Figure 5.25**b. The current density profiles in **Figure 5.25**c confirm the self-consistency of the results presented in **Figures 5.25**a and **5.25**b.

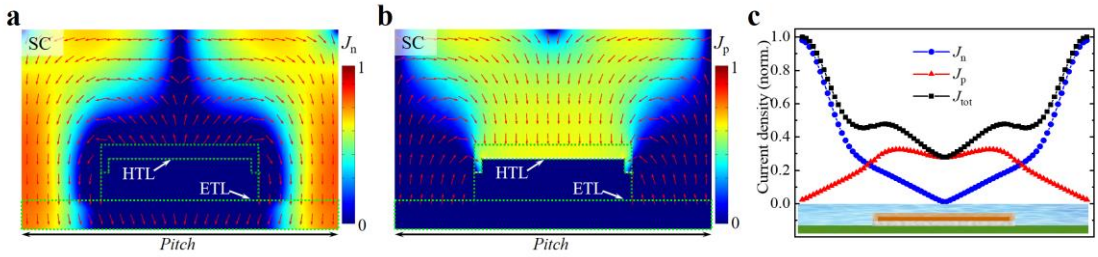

Figure 5.25 (a) J_n and (b) J_p distributions at the SC case with the corresponding directions were marked by red arrows. (c) Profiles of current densities.

Furthermore, **Figure 5.26** demonstrates the J_n and J_p at MP and OC cases, indicating reduced selectivity of charge carriers, which leads to increased charge carrier recombination losses compared to the SC case. Overall, these findings provide insights into the recombination processes and charge carrier transport mechanisms in PSCs, highlighting the importance of minimizing recombination losses for achieving higher device performance.

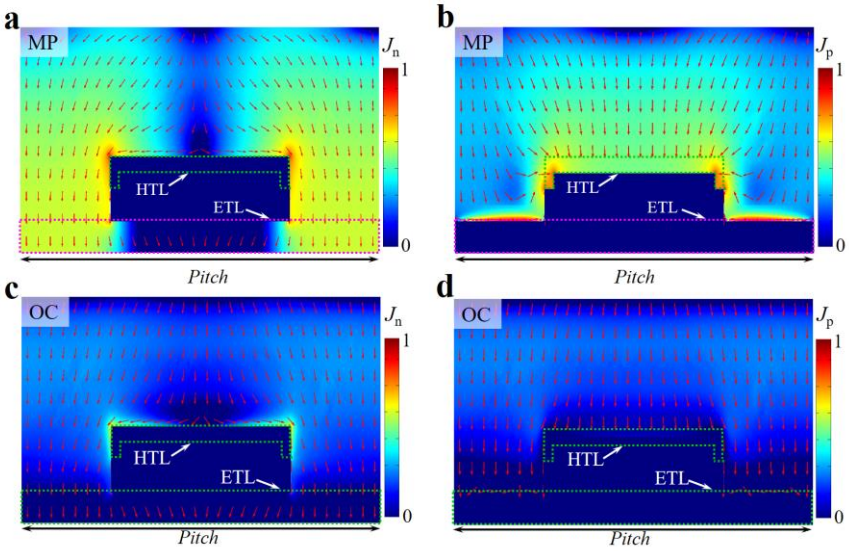

Figure 5.26 (a)/(c) J_n and (b)/(d) J_p distributions at the MP/OC case with the corresponding directions were marked by red arrows.

5.3.5 Band Offset and Material Selection

Apart from the aforementioned electrical parameters, the doping concentrations of perovskite, HTL, and ETL also influence the properties of QIBC PSCs.[183] **Figure 5.27** presents the results of N_a or N_d of the perovskite layer on cell performance.

It is evident from **Figure 5.27**a that the high performance of the two related devices, with cell efficiencies over 25%, remains relatively unchanged when N_a (N_d) is less than 10^{16} cm^{-3}. However, it significantly degrades for N_a (N_d) concentrations larger than 10^{16} cm^{-3}. The variation of J_{sc} in **Figure 5.27**b follows the same trend as the *PCE* shown in **Figure 5.27**a. Simulated *J-V* characteristic curves at representative doping concentrations in **Figure 5.27**c and **5.27**d indicate that the efficiency degradation at high doping concentrations is mainly due to increased recombination losses in the perovskite layer, resulting in decreased J_{sc}.

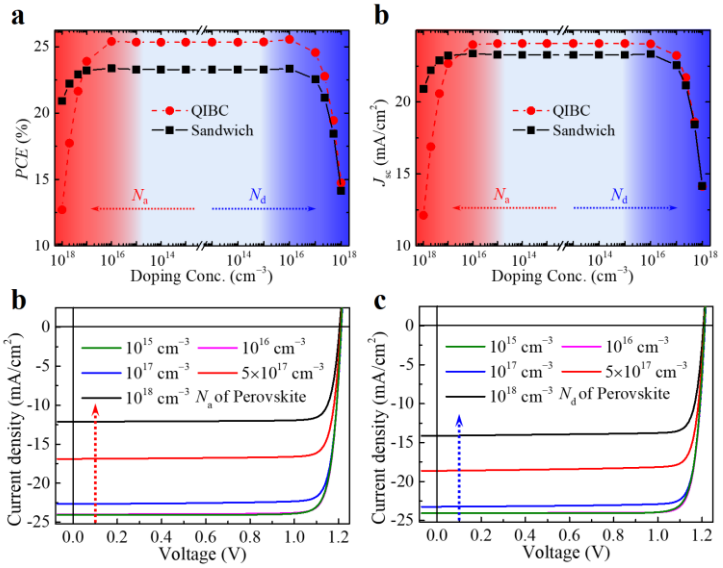

Figure 5.27 (a) *PCE* and (b) J_{sc} of the two related cases under the different doping concentrations of perovskite. (c)-(d) The representative *J-V* curves for QIBC PSCs.

Furthermore, the density of states (DOS) of the functional layers was investigated, as shown in **Figure 5.28**. **Figure 5.28**a reveals that *PCE* values first increase and then stabilize with the increase of N_d/N_c (N_a/N_v) from 10^{-5} to 1. The reduced *PCE* values for cases with relatively low N_d/N_c or N_a/N_v are primarily due to degraded *FF*, as confirmed by the *FF* variation in **Figure 5.28**b and the corresponding *J-V* curves in **Figure 5.28**c-**5.28**d. This phenomenon, where the reduced *FF* is attributed to insufficient DOS, is likely caused by increased series resistance resulting from poor hole (electron) conduction ability.[184]

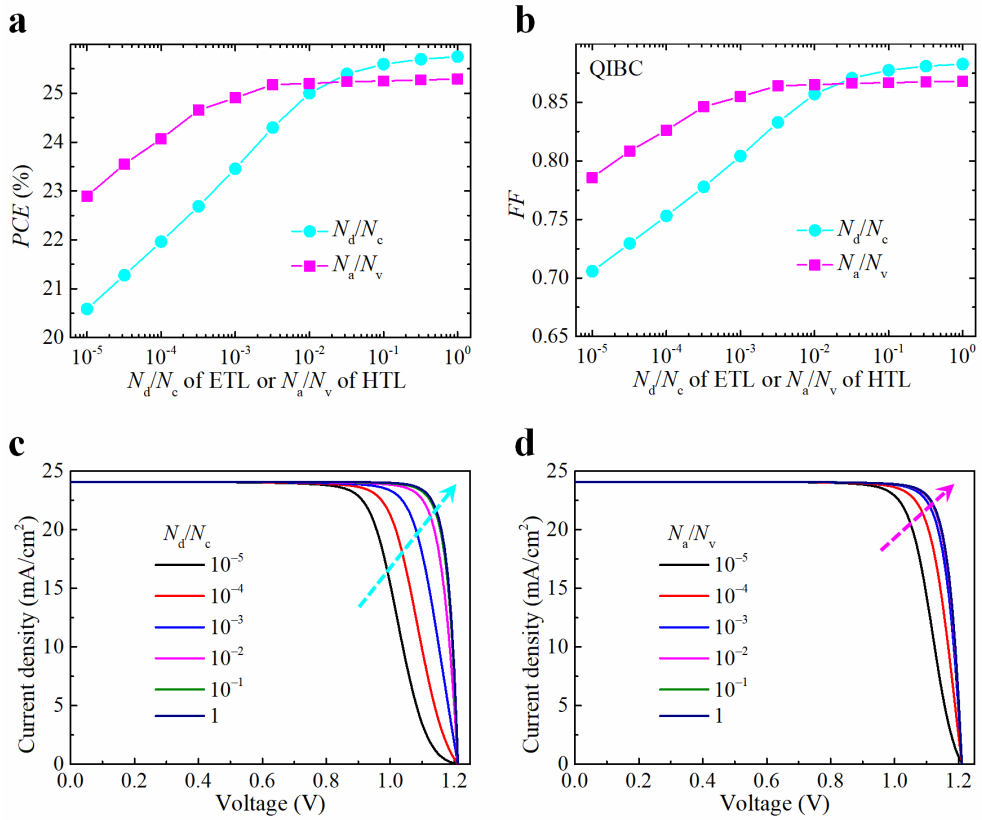

Figure 5.28 (a) *PCE* and (b) *FF* of QIBC cases as a function of N_d/N_c for ETL and N_a/N_v for HTL. (c)-(d) Representative *J-V* characteristic curves of QIBC cases. N_d/N_c (N_a/N_v) is the density of state (DOS) for ETL (HTL).

The discussions above are based on a fixed material system using SnO_2 as the ETL and NiO_x as the HTL. However, general rules that can be applied to various material systems should be discussed. To facilitate comparison, the unified material characteristics were considered by extracting the difference in conduction/valence band offset between ETL/HTL and perovskite (CBO/VBO). **Figure 5.29**a shows the CBO and VBO defined in a diagram form. Specifically, **Figure 5.29**b and **5.29**c indicate that: 1) a negative (positive) CBO with an energy cliff (spike) exists at the perovskite/ETL contact if $\chi_{ETL} < (>) \chi_{per}$, promoting/hindering electron transport; 2) a negative (positive) VBO with an energy cliff (spike) exists at the perovskite/HTL contact if $\chi_{HTL} + E_{g\_HTL} < (>) \chi_{per} + E_{g\_per}$, promoting/hindering hole transport.[185] To associate functional materials, **Figure 5.29**d shows commonly used ETL and HTL materials that have been confirmed to be effective for PSCs.[186-190]

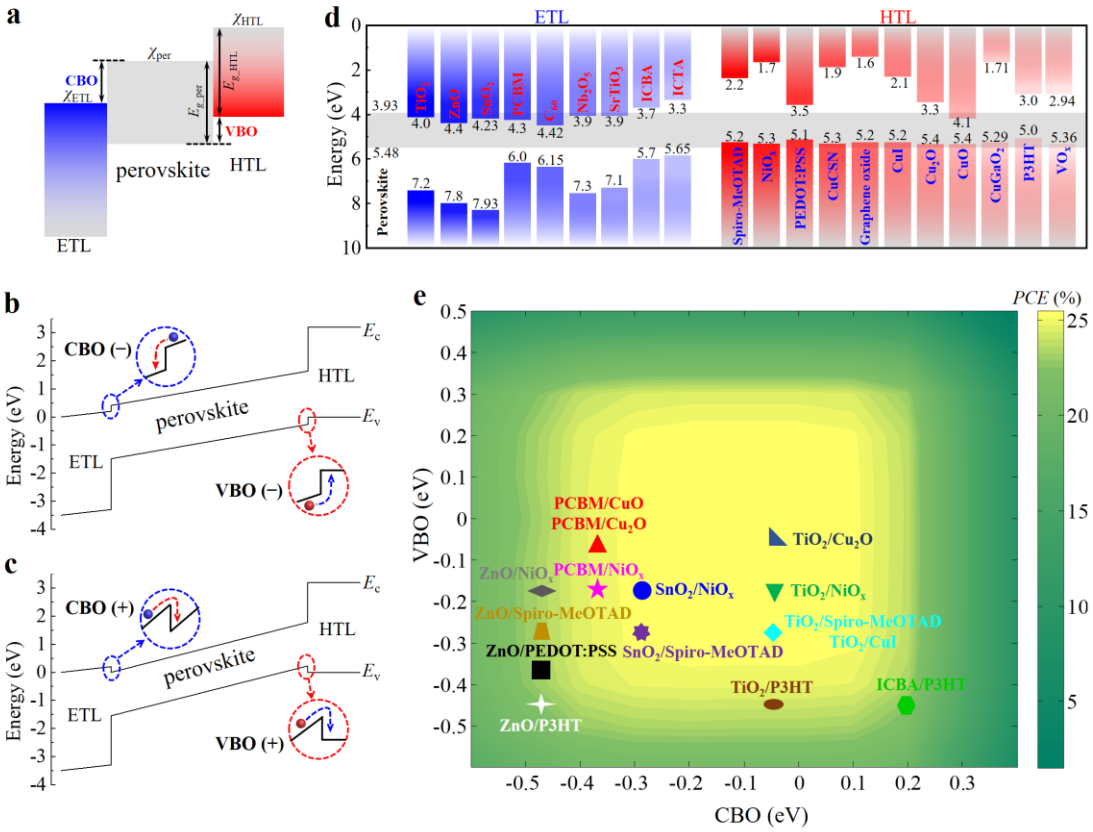

Figure 5.29 Sketch map of energy band for HTL/perovskite/ETL (a) before contact, and after contact with (b) negative and (c) positive CBO (VBO). (d) The positions of conduction and valence band for a mess of ETL and HTL. (e) *PCE* of this kind of QIBC PSCs as functions of CBO and VBO with the representative ETL and HTL groups marked in this figure.

In order to further investigate the effect of energy band positions of the ETL and HTL on device performance, the efficiencies of QIBC SCs were checked under various conduction band offsets (CBO) and valence band offsets (VBO), as shown in **Figure 5.29**e. It is evident that high device performance can be expected within suitable ranges of CBO and VBO, specifically, −0.4 eV < CBO < 0.2 eV and −0.4 eV < VBO < 0.3 eV. For a high positive CBO/VBO, the formation of an energy barrier for electrons/holes at the ETL/HTL and perovskite interface would degrade device performance. On the other hand, a high negative CBO/VBO promotes carrier transport due to the formation of a cliff. However, a large CBO/VBO would increase carrier recombination losses at the interfaces, leading to degraded device performance due to adverse activation energy.

Additionally, **Figure 5.29**e marks a variety of ETL and HTL materials that have been widely reported by others, along with the corresponding *PCE* values summarized in **Table 5.2**.

Table 5.2 Summary of *PCE* for the various ETL/HTL designs.

ETL/HTL designs	CBO (eV)	VBO (eV)	*PCE* (%)
PCBM/CuO or PCBM/Cu_2O	-0.37	-0.08	24.71
TiO_2/Cu_2O	-0.07	-0.08	25.50
ZnO/NiO_x	-0.47	-0.18	22.95
PCBM/NiO_x	-0.37	-0.18	24.69
SnO_2/NiO_x	-0.30	-0.18	25.32
TiO_2/NiO_x	-0.07	-0.18	25.47
ZnO/Spiro-MeOTAD	-0.47	-0.28	22.93
TiO_2/Spiro-MeOTAD or TiO_2/CuI	-0.07	-0.28	25.40
ZnO/PEDOT:PSS	-0.47	-0.38	22.65
SnO_2/Spiro-MeOTAD	-0.30	-0.28	25.30
ZnO/P3HT	-0.47	-0.48	21.45
TiO_2/P3HT	-0.07	-0.48	23.44
IBCA/P3HT	0.23	-0.48	21.97

5.3.6 Ion Migration Effect

Ion migration of perovskite, which has been widely reported, is responsible for the hysteretic *J-V* curves[191] and the degradation of perovskite.[192] This section investigates the impact of ion migration on the properties of QIBC PSCs. In the presence of mobile ions in the perovskite layer, the distribution of electric field intensities and free charge carriers will be modified, thereby mediating the charge carrier transport process and affecting the photoelectric properties of the devices. The simulated equations and simulation details were presented in Chapter 2 (2.1.3 Ion Migration), enabling a

thorough investigation based on a 2D model. In this simulation, the degeneration of perovskite, which is difficult to monitor, was neglected.

For cases without ion migration, cations and anions inside the perovskite films remain unseparated. However, in cases with ion migration, anions and cations separate and travel to their respective contacts driven by the built-in electric field, ultimately accumulating near the perovskite interfaces. This accumulation of ions near the perovskite interfaces influences the built-in electric field, adjusts the energy alignment, regulates carrier transport, and affects the cell efficiencies. The influence of ion concentration (N_i) inside the perovskite layer on cell efficiencies was investigated in **Figure 5.30**. The results indicate that for cases with low N_i ($N_i < 10^{16}$ cm^{-3}), ions inside the perovskite layer have almost no effect on cell efficiencies. However, for cases with relatively high N_i ($N_i > 10^{16}$ cm^{-3}), ions inside the perovskite layer degrade cell efficiencies.[193] Therefore, it is necessary to suppress N_i to some degree in order to achieve high-efficiency QIBC PSCs.

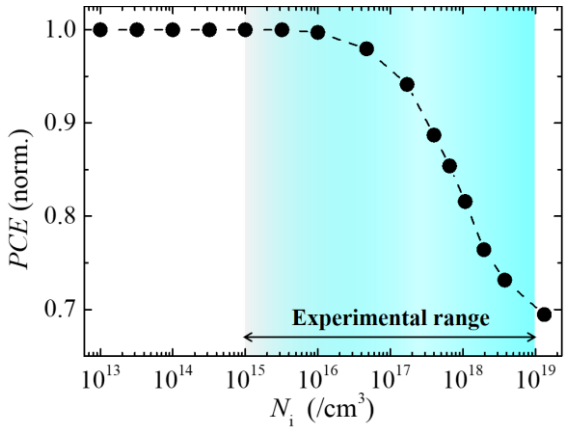

Figure 5.30 Normalized *PCE* under the various N_i.

To further understand the physical mechanism of QIBC PSCs with mobile ions, a comprehensive investigation was conducted, including energy band diagrams, distributions of free carrier/ion concentrations, and space-charge densities (ρ), as shown in **Figure 5.31**a-**5.31**c. Three cases with different N_i concentrations (0, 10^{15} cm^{-3}, and

10^{17} cm^{-3}) were considered. For the case with a low N_i concentration of 10^{15} cm^{-3}, there is no significant difference in energy levels compared to the case with $N_i = 0$. However, as N_i increases to 10^{17} cm^{-3}, the energy levels of the conduction and valence bands become flatter inside the perovskite region due to the accumulation of ions at the perovskite-related interfaces. This is supported by the spatial potential distributions shown in **Figure 5.32**.

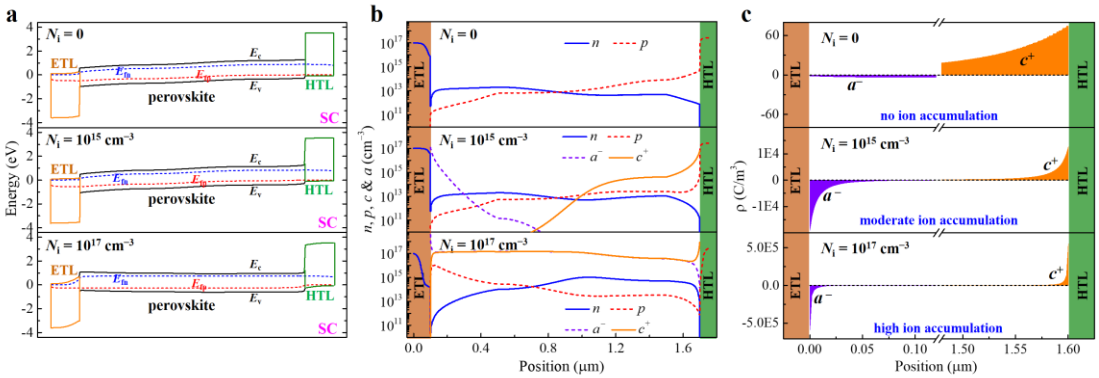

Figure 5.31 (a) Energy band levels, (b) concentrations of free charge-carriers together with ions, and (c) space-charge densities (ρ) of this kind of QIBC PSCs at three representative N_i.

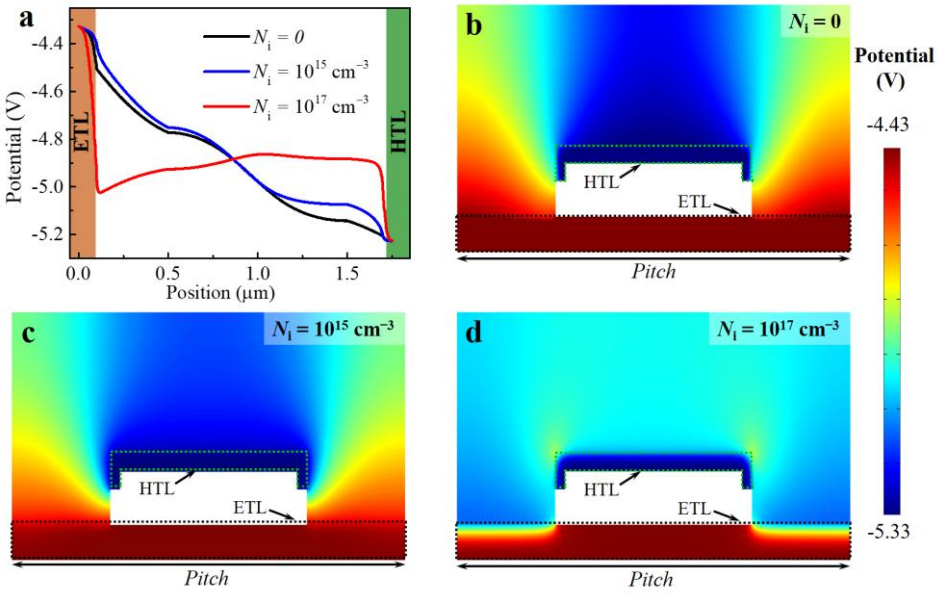

Figure 5.32 Position-dependent and 2D profiles of potentials under three typical cases.

The distributions of free charge carriers and ion concentrations shown in **Figure 5.31**b

reveal the following: 1) for a moderate N_i concentration of 10^{15} cm^{-3}, the concentrations of cations and anions exponentially decrease from the surface to the bulk, and the concentrations of free charge carriers are minimally affected by ions; 2) for a high N_i concentration of 10^{17} cm^{-3}, the concentrations of ions show a rapid increase followed by leveling off, and the concentrations of free charge carriers exhibit significant changes due to the presence of ions. More specifically, the 2D profiles of ion distributions for $N_i = 10^{17}$ cm^{-3} are shown in **Figure 5.33**, indicating that the anion (cation) concentration is strengthened at the ETL/perovskite (HTL/perovskite) interface.

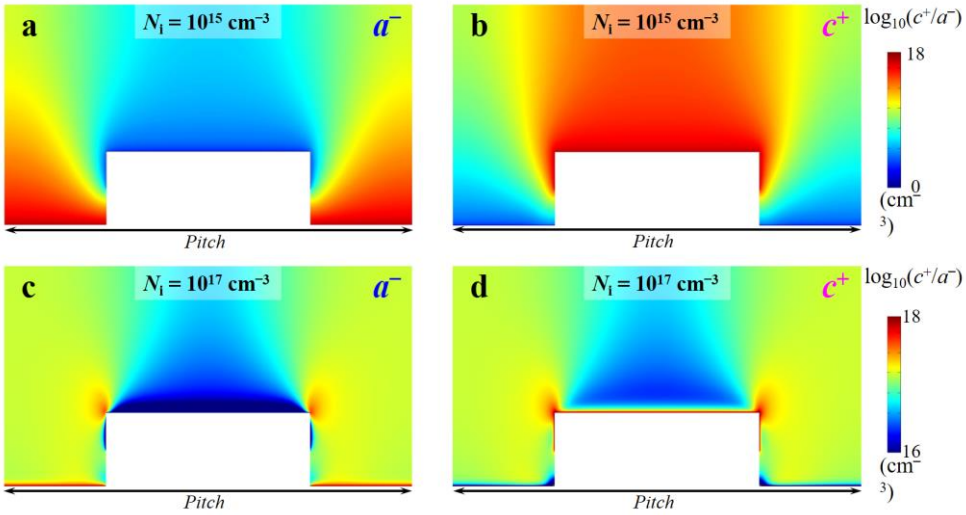

Figure 5.33 Concentration profiles of anions and cations under $N_i = 10^{15}$ cm^{-3} and 10^{17} cm^{-3}.

Moreover, the corresponding ρ distributions for the three cases demonstrate that the accumulations and depletions of both anions and cations at the surfaces, especially for the case with a N_i concentration of 10^{17} cm^{-3}, are mainly restricted to the relatively narrow Debye layer. The accumulation of these ions at the surface of the perovskite layer is the main reason for the changes in energy band offset, carrier concentration, and potential distribution, which undoubtedly affect the device efficiencies as shown in **Figure 5.30**.

5.3.7 Photon Recycling Effect

For PSCs, especially QIBC PSCs, limited carrier diffusion lengths can impede carrier transport and lead to increased recombination within the perovskite layer. Photon recycling (PR) is a process that reuses emitted photons through absorption, diffusion, and re-emission, thereby promoting carrier diffusion lengths and suppressing radiative recombination. By incorporating the PR effect, the quasi-Fermi level splitting in the perovskite layer can be enhanced, resulting in increased V_{oc} and *PCE*.

It has been widely demonstrated that PR has a positive impact on PSCs, which is also applicable to QIBC PSCs in principle. Numerical simulations were performed to investigate PR, with the simulation details introduced in Chapter 2 (2.1.4 Photon Recycling). The PR, P_a, and P_e values were obtained as shown in **Figure 5.34**a. It is evident that as the fill factor (*ff*) increases, P_e increases while P_a and P_r decrease.

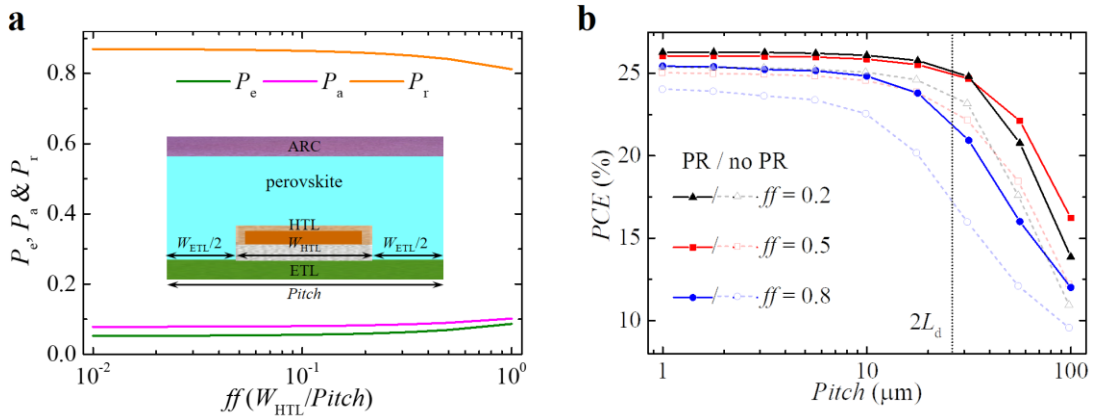

Figure 5.34 (a) Proportions of P_r, P_a and P_e under the various *ff*. (b) *PCE* values for QIBC PSCs under the various *Pitch* for the two related cases.

Figure 5.34b presents the *PCE* results for various pitches ranging from 1 μm to 100 μm. In this analysis, surface recombination losses at the ETL/perovskite and HTL/perovskite interfaces were significantly suppressed with a low D_{it} of 10^8 cm^{-2}, enabling the study of PR effects conveniently. From **Figure 5.34**b, the following conclusions can be drawn: 1) for all *ff* values, PR has a positive effect on device

performance, resulting in higher *PCE*, particularly for larger *pitches*; 2) for all *ff* values, device performance remains relatively stable for smaller *pitches* (< 5 μm), but significantly decreases for larger *pitches*; 3) in the presence of PR, the highest *PCE* values were achieved at *ff* = 0.5, suggesting an optimal balance between hole and electron transport. **Figure 5.35**a and **5.35**b demonstrate the *PCE* of QIBC PSCs as functions of *pitch* and carrier diffusion length (L_d). It is evident that in the presence of PR, QIBC PSCs exhibit higher tolerance to pitch and L_d variations, resulting in higher *PCE* values compared to devices without PR. This implies that the inherent poor *PCE* observed in non-PR devices can be mitigated by incorporating PR. Additionally, **Figure 5.35**c-**5.35**d illustrate the distributions of recombination components for the two corresponding cases. Clearly, the proportion of radiative recombination decreases from 89% to 68% with the inclusion of PR.

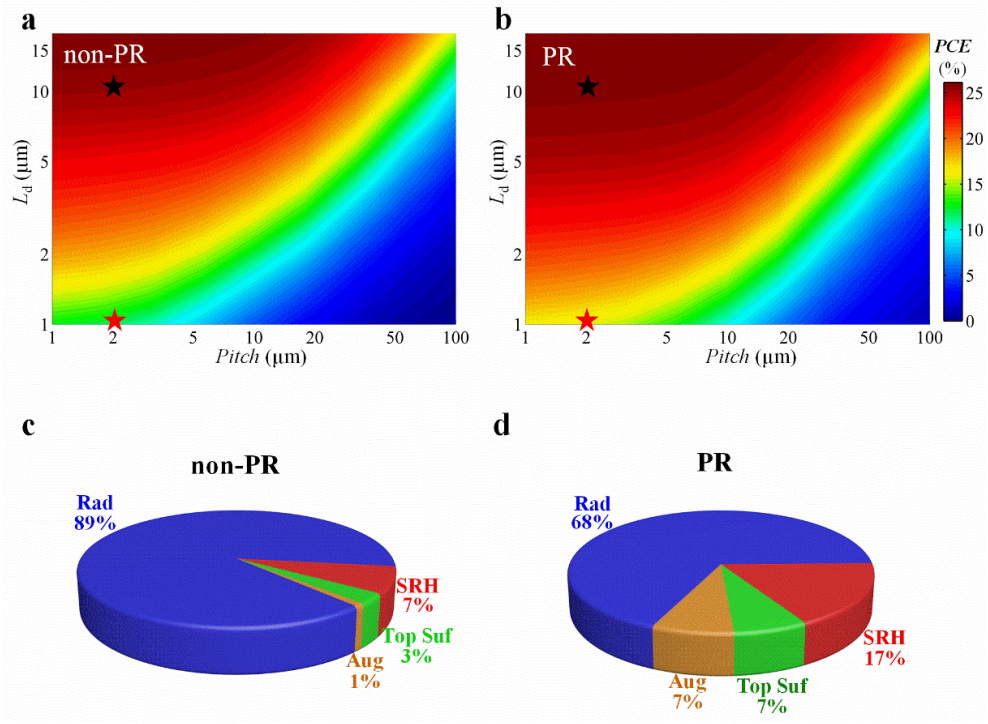

Figure 5.35 (a)-(b) *PCE* as functions of L_d and *Pitch* for two related cases with (c)-(d) the corresponding loss distributions.

The light *J-V* characteristic curves of two representative samples with L_d values of 1 μm and 10 μm are presented in **Figure 5.36**a. The following conclusions can be drawn:

1) for the case of L_d = 1 μm, the QIBC PSCs without PR exhibit a typical S-shaped *J-V* curve due to increased SRH recombination. However, the introduction of PR mitigates this effect; 2) for the case of L_d = 10 μm, SRH recombination is effectively suppressed, and ideal *J-V* curves are observed, with the PR case achieving a higher V_{oc}.[194] This conclusion is supported by Equation 5.3, which demonstrates that decreasing J_{0rad} leads to an improved V_{oc}.

$$V_{oc} = \frac{k_B T}{q} \ln\left(\frac{J_{sc}}{J_0^{rad} + J_0^{nrad}} + 1\right) \tag{5.3}$$

where J_0^{rad} (J_0^{nrad}) is the saturation currents due to radiative (nonradiative) recombination. Furthermore, a detailed technical roadmap for enhancing *PCE* is proposed in **Figure 5.36**b, revealing the following: 1) by further reducing recombination losses from Auger and SRH processes, the device efficiency can be boosted to 25.8%; 2) the inclusion of PR enables achieving a high efficiency of 27.2%; 3) through optical optimization, this type of QIBC PSCs is expected to reach a *PCE* of 29.9%. The corresponding *J-V* curves are shown in **Figure 5.36**c.

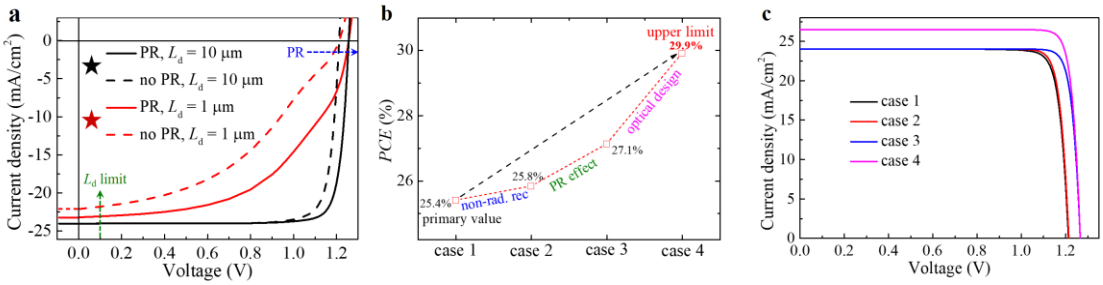

Figure 5.36 (a) Light *J-V* characteristic curves of QIBC devices for the two related cases. (b) Roadmap for *PCE* promotion. (c) The corresponding light *J-V* curves in figure 5.36b.

It is worth noting that despite the high radiative recombination, the predicted maximum *PCE* of 29.9% for QIBC PSCs still falls short compared to conventional PSCs, which are predicted to reach a higher *PCE* of 31%.[44] In summary, a feasible roadmap is provided to achieve high-efficiency QIBC PSCs.

5.3.8 Conclusion

A comprehensive model combining traditional photoelectric models for free carriers, ion models, and PR models was developed for QIBC PSCs to accurately simulate the carrier generation, transport, and recombination processes. The simulation results indicate that QIBC PSCs can achieve higher current density compared to conventional sandwich PSCs, thanks to reduced parasitic absorption losses. By optimizing parameters such as passivation quality, mobility, and doping concentration, a cell efficiency exceeding 25% is predicted. Mobile ions within the perovskite layer significantly impact cell efficiencies, particularly when $N_i > 10^{16}$ cm^{-3}, as they modify energy band levels, charge-carrier distributions, and the electric field. Additionally, the study highlights the positive impact of PR on QIBC PSC properties, as the introduction of PR effectively enhances V_{oc} and *PCE*.

Chapter 6 Conclusions and Outlook

6.1 Conclusions

This thesis introduces advanced simulation technologies coupled with well-designed experiments to elucidate the charge-carrier transport mechanism and propose an efficiency improvement roadmap for c-Si and perovskite solar cells. The main research content is divided into three sections: Si-based IBC SCs, TOPCon SCs, and perovskite SCs.

In Chapter 3, the design principles and related mechanisms for dopant-free c-Si IBC SCs are explored through experiments and simulations. Using PEDOT:PSS as the HTL and MgO_x as the ETL, the impact of fill ratio, pitch, and surface recombination velocity on the properties of IBC SCs is investigated. Recombination distributions are analyzed, revealing that strong recombination losses at the ETL/Si surface are responsible for poor device performance. The charge-carrier transport mechanism is clarified by examining the distributions of carrier currents and electric fields. It is found that optimizing the ETL/Si interface can lead to a high efficiency exceeding 24%.

Furthermore, an advanced method is proposed for passivating the front surface of Si by utilizing fixed charges inherent to dielectric layers. Numerical simulations confirm the effectiveness of this approach for IBC c-Si SCs. The electric field induced by inherent charges on the front-side of the Si surface facilitates the transport of bulk carriers and reduces recombination losses at both the front-side and rear-side interfaces. Simulated results indicate that a high *PCE* can be achieved when the front-surface charge is larger than 5×10^{12} cm^{-2} or when the front-surface is well-passivated with $D_{it} < 10^{10}$ $eV^{-1}cm^{-2}$. Additionally, negative charges exhibit slightly higher *PCE* than positive charges when $Q_f > 10^{12}$ cm^{-2} due to higher potential and stronger electric fields. The energy band, potential, electric field, and carrier concentration distributions near the front-surface are

analyzed to explain the increment in *PCE*. The front-surface charge also positively impacts the bulk-Si region, promoting carrier transport throughout the Si region and partially suppressing recombination losses at the HTL/*n*-Si, ETL/*n*-Si, and gap/*n*-Si interfaces by strengthening the electric field.

Similarly, the method of using electric-field induced by inherent charges in the dielectric layers to passivate the rear-side gap region is investigated. The impact of Q_f and S_{gap} on the device properties of IBC SCs is examined through numerical simulations. It is revealed that outstanding device performance with high *PCE* can be achieved when $|Q_f| > 10^{12}$ cm^{-2} or $|Q_f| < 10^{11}$ cm^{-2}. The simulation results show that positive fixed charges result in higher *PCE* than negative fixed charges if $|Q_f|$ is less than 2×10^{11} cm^{-2}. However, negative fixed charges can achieve excellent *PCE* if $|Q_f|$ is larger than 5×10^{11} cm^{-2}. For poor gap passivation ($S_{gap} = 10^3$ cm/s), reducing the gap size (f_{gap}) can improve the *PCE* of this type of IBC-HJ SC, but it cannot completely suppress carrier recombination losses, even with a small f_{gap}. Electric field and carrier current density distributions are analyzed to elucidate the carrier transport mechanism. The gap fixed charges can also impact the passivation quality of other related interfaces (ETL and front surface) in cases of poor passivation. Moreover, rear gap negative fixed charges with high Q_f exhibit a high tolerance to ETL thickness and *pitch* size. The displayed results and passivation mechanism provided a simple and a feasible approach in developing IBC SCs with high efficiencies.

In Chapter 4, detailed simulations and experiments were conducted to investigate the dynamics of contacts with pinholes in the local region, including the mechanism of charge-carrier transport and the formation process of pinholes. Through TEM and c-AFM measurements, it was confirmed that local SiO_x fracture with the presence of pinholes occurs, and the pinhole density was determined. The formation of pinholes was analyzed by studying the dynamics during high-temperature annealing, suggesting that stresses resulting from thermal expansion are responsible for the fracture of SiO_x films. Numerical simulations helped address the carrier transport mechanism for poly-

$Si/SiO_x/Si$ contacts, indicating that carrier transport occurs through a competition between tunneling and direct transport through pinholes. The dominant behavior is determined by the size/density of pinholes and the thickness of SiO_x films. Passivation and contact properties of this contact were studied through experiments and a foundational physical model. Proof-of-concept devices with complete cell structures were fabricated, suggesting that the combined effect of passivation and contact properties yields the best response in terms of device efficiencies. Additionally, a detailed current-recombination analysis and prediction of device efficiencies were carried out, indicating a special approach to boost the efficiencies of this type of TOPCon SCs to 27%.

In Chapter 5, a novel optical design for PSCs was proposed, involving the texturing of the front-side glass using a gradient-index Gaussian-type structure. Numerical simulations showed that this design exhibited a broadband light-harvesting response, resulting in a remarkable photocurrent density of 23.35 mA/cm^2, which was 1.21 mA/cm^2 higher compared to the normal design with a current value of 22.14 mA/cm^2. The optical absorption and loss distributions were analyzed, indicating that the Gaussian-type structures effectively reduced reflection losses, resulting in a decrease of 2.55 mA/cm^2 compared to 3.93 mA/cm^2 for flat structures. The optical management mechanism was clarified by examining the electric-field distributions. Furthermore, PSCs with the Gaussian-shaped profile demonstrated outstanding optical response, even with varying perovskite thicknesses and incident angles.

By combining the traditional photoelectric model of free charge-carriers with ion and PR models, a comprehensive model was developed to simulate the carrier generation, transmission, and recombination process of QIBC PSCs. The simulation results revealed that QIBC PSCs can provide higher current density compared to ordinary sandwich PSCs due to a reduction in parasitic absorption loss. By investigating electrical parameters such as passivation quality, mobility, and doping concentration, it was predicted that cell efficiency could exceed 25% under optimized parameters. The

presence of mobile ions in the perovskite layer had a significant effect on cell efficiencies, particularly when the N_i was greater than 10^{16} cm^{-3}, as the mobile ions could alter the energy band, free carrier distribution, and spatial electric field. Additionally, the effect of PR on the properties of QIBC devices was studied, revealing that the introduction of PR can effectively enhance the V_{oc} and *PCE* of QIBC PSCs.

6.2 Outlook

For dopant-free IBC c-Si solar cells, there is a great potential to surpass traditional doped solar cells in terms of device efficiencies. Moreover, this technology is simpler and more popular in terms of manufacturing. However, the main challenge lies in the overall efficiency of dopant-free IBC c-Si solar cells, which currently falls below 24%. This is lower than the highest efficiency achieved by traditional high-efficiency c-Si solar cells at 26.7%. The primary reason for the low device efficiency is poor interface passivation, despite various attempts to improve passivation quality in related interfaces. The following schemes are proposed to enhance interface passivation and device efficiency:

1) Utilize high-quality passivation materials for interfaces, such as SiO_x and a-Si:H(*i*). However, the introduction of these dielectric passivation layers may increase overall contact resistance to some extent. Therefore, it is necessary to minimize the negative impact caused by contact resistance through the adjustment of thickness and impurity doping, striking a balance between passivation and contact performance.

2) Improve the quality of functional layers (*e.g.*, electron-transport layer/ hole-transport layer) or develop new material systems. These functional layers should simultaneously meet several requirements, including low/high work function for electron-transport layer/hole-transport layer, low bulk resistance and contact resistance, good Ohmic contact with corresponding electrodes, and low parasitic absorption.

3) Optimize the structural size. Based on high-level passivation, optimizing the size and proportion of the hole-transport layer, electron-transport layer, and gap can

potentially achieve the best device efficiency.

In summary, obtaining high-efficiency dopant-free IBC c-Si solar cells remains a challenging task, despite their significant potential.

Regarding TOPCon solar cells, this technology has experienced rapid development in the past decade, and mass production is on the horizon. However, to enhance the competitiveness of TOPCon technology, further improvements in device efficiencies are necessary. Although the current maximum efficiency has reached 26%, further advancements are increasingly difficult to achieve. Therefore, it is essential to deepen the understanding of the physical mechanisms underlying TOPCon technology and strike a balance between contact and passivation properties of the poly-Si/SiO_x/c-Si contact. The next focus areas can be summarized as follows:

1) Elucidate the carrier transport and passivation mechanism of pinholes on textured c-Si substrates.

2) Balance passivation and contact properties through optimization of annealing time/temperature, SiO_x thickness, and impurity doping.

3) Enhance the passivation quality of SiO_x to achieve the highest level of passivation.

4) Suppress optical parasitic absorption and improve photocurrent response.

5) Optimize the design of the front-side contact.

In conclusion, TOPCon solar cells hold promise as the mainstream technology in the PV community due to their advantages in terms of module cost and device efficiency.

When it comes to PSCs, two approaches have been proposed to enhance cell performance: the Gaussian-type structure and the QIBC design. Both approaches aim to improve photocurrent and efficiency by minimizing reflection. However, implementing these schemes in practice can be challenging. Advanced optical designs face difficulties in experimentally achieving the optimal size determined through simulations. The optical performance is highly sensitive to structural size, and even slight differences can significantly impact device performance. Therefore, it is

necessary to further develop feasible optical structures with larger tolerances to variations in size, such as multilayer designs.

Regarding QIBC PSCs, reported efficiencies are relatively low, primarily due to challenges in the integration process. Integrating both types of transport layers on the rear of the devices increases the difficulty of device integration and affects the quality of the transport layers and perovskite films. The carrier diffusion length in the perovskite film is generally shorter than that of c-Si, requiring a smaller pitch size. Additionally, PSCs with thin films of only a few hundred nanometers cannot withstand high-temperature processes, further complicating the integration of highly efficient devices. Therefore, key factors in achieving high-efficiency QIBC PSCs include the development of small-size back electrodes and the fabrication of high-quality perovskite films and functional materials.

In summary, there is still a long way to go in preparing high-efficiency QIBC PSCs. This involves screening and optimizing suitable passivation and functional materials, improving preparation technologies, and designing advanced structures. Once these challenges are addressed, the concept of QIBC PSCs is expected to significantly enhance their competitiveness in the field of photovoltaics.

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