Soft-Start procedure for a three-stage smart transformer based on dual-active bridge and cascaded H-Bridge converters

Pugliese, S., Buticchi, G., Mastromauro, R.A., Andresen, M., Liserre, M., Stasi, S.

University of Nottingham
UK | CHINA | MALAYSIA

University of Nottingham Ningbo China, 199 Taikang East Road, Ningbo, 315100, Zhejiang, China.

First published 2020

University of Nottingham
UK | CHINA | MALAYSIA

Soft-Start Procedure for a Three-Stage Smart Transformer based on Dual Active Bridge and Cascaded H-Bridge Converters

S. Pugliese, *Member, IEEE*, G. Buticchi, *Senior Member, IEEE*, R. A. Mastromauro, *Senior Member, IEEE*, M. Andresen, *Member, IEEE*, M. Liserre, *Fellow, IEEE*, and S. Stasi

***Abstract*— Power electronics-based three-stage smart transformers (ST) can be seriously damaged by inrush currents and overvoltages during the start-up phase if the control of the stages is not correctly coordinated. Hence, it is crucial to design properly the start-up procedure, especially in case of modular architectures with distributed DC-links. The design of the start-up procedure depends on the ST power stages topologies, their control systems and the operation modes. This work proposes a soft-shift start modulation technique that allows to limit the inrush current in the DC/DC isolation stage during the DC-link capacitors pre-charging. A fast voltage balancing control, performed by the DC/DC isolation stage, is introduced to avoid overvoltages and unbalanced voltage conditions among the different power cells. Under the proposed method, fast control dynamics is guaranteed thanks to the high frequency bandwidth of the DC/DC isolation stage converters. Theoretical analysis, based on a detailed small signal model of the ST, and simulations are used to demonstrate the principle of the operation. Experimental results, carried out in a ST prototype, confirm the performances of proposed solution in realizing a smooth start-up without voltage/current overshoots.**

***Index Terms*— Soft-Start Procedure, Smart Transformer, Cascaded H-Bridge Converter, Dual Active Bridge Converter.**

I. Introduction

The smart transformer (ST) is an intelligent distribution substation based on the power electronics which can be implemented on the basis of a solid state transformer (SST) or on the basis of a back-to-back converter plus a standard transformer. In the framework of smart grids, the ST concept has recently attracted the attention of industry for the capability to regulate the voltage, the frequency, the active and reactive power flow, and to allow meshed-operations of distributed feeders [1-6]. Considering the modular three-stage ST based on the cascaded H-bridge (CHB) converter and the dual active bridge (DAB) converters in Fig. 1, the paper focuses on the start-up procedure which has to be coordinated with the specific control system.

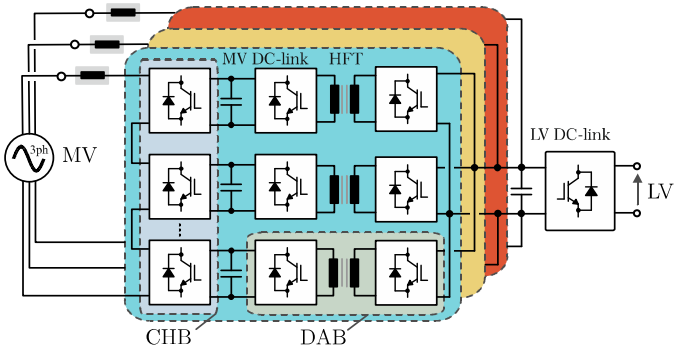

Fig. 1. CHB and DAB converters in three-stage ST modular architecture.

Examining previous literature about STs based on CHB and DAB converters, the design results in multiple control objectives, whereby the MV DC-link voltages of the power conversion cells can be balanced either by the AC/DC stage control [7-9] or by the DC/DC power conversion stage [10-12].

In case the MV side AC/DC converter is in charge of the MV DC-link voltage balancing control, it allows to employ conventional control strategies already developed for the CHB converter standalone applications. Differently, in [10-11], it is demonstrated that the MV DC-link voltage balancing operated by the DC/DC power conversion stage provides improved dynamic performances. In the present paper, it is proven that the MV DC-link voltage balancing technique presented in [10] is particularly advantageous in order to optimize the start-up operation of modular three-stage STs.

Few studies have been previously addressed on the start-up procedure of the ST. In [13] a preliminary start-up procedure is

This work was supported in part by the European Union/Interreg V-A Germany-Denmark, under PE:Region Project, in part by the European Research Council under the European Union's Seventh Framework Programme (FP/2007-2013)/ERC Grant Agreement n. [616344] - HEART and in part the Ningbo Science & Technology Bureau under Grant 2013A31012 and NSFC under Grant 51650110507. Corresponding author: Sante Pugliese, Christian-Albrechts-Universität zu Kiel, Chair of Power Electronics, Kiel, Germany (sapu@tf.uni-kiel.de).

S. Pugliese, M. Andresen and M. Liserre are with the Chair of Power Electronics, Christian-Albrechts Universität zu Kiel, Kiel 24143, Germany (e-mail: sapu@tf.uni-kiel.de; ma@tf.uni-kiel.de; liserre@ieee.org).

G. Buticchi is with the Faculty of Science and Engineering, University of Nottingham Ningbo China, Ningbo 315100, China (email: Giampaolo.Buticchi@nottingham.edu.cn).

R. A. Mastromauro is with the Department of Information Engineering, University of Florence, Florence 50139, Italy (e-mail: rosaanna.mastromauro@unifi.it).

S. Stasi is with the Department of Electrical and Information Engineering, Politecnico di Bari, Bari 70125, Italy (e-mail: silvio.stasi@poliba.it).

presented considering a non-modular ST configuration, but it has to be highlighted that the start-up procedure depends on the ST architecture, the operation modes like grid feeding and grid forming and the control systems. The first studies related to the start-up of modular three-stage STs, and based on a stage-by-stage procedure, are proposed in [14-16]. In all these cases conventional control structures are adopted.

Recent studies such as [17] and [18] tackle the start-up procedure by focusing on the energization issue based on the use of auxiliary power units (APUs). In all these studies, parameter and/or voltage imbalance conditions during the start-up procedure are not considered and, in conclusion, it is recognized that the fundamental task in the start-up procedure is operated by the AC/DC power stage more than the DC/DC power stage.

More recent studies are focused on the role of the DC/DC power stage; in particular, considering a traction three-stage power electronic transformer based on CHB and DAB converters, in [19], a voltage-balance-based control applied to the DAB converters is proposed under parametric/voltage unbalanced conditions. Nevertheless, the system does not provide inrush current control of each single DAB converter and inrush stress-current sharing between different DABs.

Differently, in [20] a combination of model predictive control with current stress optimization scheme allows to achieve high dynamics performance in the output voltage regulation together with self-power balancing of the output parallel DAB converters. The control scheme could support the ST start-up procedure, but start-up issues are not treated in the paper.

Considering the same ST topology, in [12] DAB converters are in charge of the LV DC bus voltage control, the power balance and the MV DC-links voltage control. Nevertheless neither details about the design of the control system nor results in case of voltage or power imbalances are provided in the paper. Besides parameters mismatches are not considered in [12].

In [21] it is analyzed the inrush current issue deriving from the transition in case of a power module failure. The low-voltage DC-link of the redundant power module is charged by a dedicated charging controller providing constant current to the power module. The focus is on redundancy achievement and not start-up operation. The control method used in [21] cannot be directly extended to the start-up procedure of a ST avoiding modifications.

Finally in [22] it is tackled the start-up of some DAB converters connected to a PV source. The proposed topology is not a ST but a two-stage architecture which is energized by the LV DC side and not by the MV AC side. Besides in [22] conventional controllers are adopted, no details about the design procedure are provided and dynamics issues are not tackled.

Considering the configuration in Fig. 1, the paper proposes a start-up procedure for a modular three-stage ST energized from the MV AC side. The pivotal role is performed by the DC/DC power conversion stage which is in charge of the voltage balancing among the MV DC-links and of the inrush overcurrent limitation in the high frequency transformers (HFTs). A soft-start procedure, based on a modified modulation technique of the DAB converters, provides the aforementioned HFT overcurrent limitations. The main focus is on the first two stages of the ST since, as in [10], the proposed architecture is conceived to be coupled with DC smart grids. The soft-start procedure avoids the use of any APU and it is tailored considering the overall control system. The control system is based on the theoretical model of the ST taking into account voltages imbalance conditions.

The rest of the paper is organized as follows: in Section II the main ST start-up and control issues are discussed, Section III deals with the mathematical model of the ST and the balance control design; Section IV describes the soft-start procedure, Section V presents the experimental results and finally Section VI concludes the paper with some remarks.

II. ST Start-up And Control Issues

ST start-up implies a soft-start procedure where two important conditions need to be satisfied:

1) Balancing of the DC-link voltages in the MV side;
2) Soft-charging of the capacitors in the LV side;

However, it should be considered that, due to the mismatch of MV DC-link capacitors parameters, voltage imbalance problems cannot be avoided. If a voltage balance control is not adopted, the deviation of the voltages (and/or currents) may become larger than the IGBT blocking voltage limit and finally it may results in the failure of the IGBTs and/or of the DC-link capacitors. Therefore it is very important to balance the voltage in the ST DC-links in transient operation like the start-up procedure as well as in steady-state.

A. Balancing of the DC-link voltages in the MV side

In literature there are many kinds of voltage balancing strategies, but they can be essentially classified into two categories [19]:

1) the CHB and the DABs are controlled independently; this means that the voltage balance control in MV is demanded from the CHB stage, while the DAB converters control the output voltage in the LV side [23];
2) the ST is controlled as a single converter. Hence, the MV balancing control is demanded from the DABs together with the voltage control in LV side. A power balance control approach can be adopted by the CHB, to level out the stress in each cell [11] and [24].

The first voltage balancing strategy is the most used [9], but it usually presents a slower dynamic response due to the low switching frequency at which the CHB is normally operated. Furthermore, the CHB control may require modifications to ensure the balancing in all conditions, whereas the DAB solution can freely route the power through the LV DC-link.

The traditional start-up procedure matches with the first ST control approach. It operates the voltage balance in the CHB converter, which starts as first, followed by the DAB converters. Using this procedure, overvoltage and capacitors or IGBTs failures can occur since the CHB control performance depends on the initial conditions of each cell, as discussed in [25-26]. In particular, due to the mismatch of the MV resistance

and capacitance parameters, the steady-state voltages reached by each DC-link of the CHB in grid-connected passive rectifier operation, are quite different among them. Hence, the initial state in each DC-link is different from the others and the voltage balancing cannot be achieved before the CHB converter starts. In such nonlinear systems, the behavior of the controlled variables during the start-up, depends on its own values in the initial condition [25-26]. Usually the control design workflow for the CHB converter is realized considering a linearized model of the control in the steady-state conditions but, in case of a wide voltage range of operation, such a linearized model does not represent the real dynamics anymore, as it happens during the soft-start. Different initial conditions, such as unbalanced DC-link voltages, could give rise to unpredictable voltages behavior and it can lead to unstable operation.

Referring to the power stage parameters of a 5-level CHB converter as reported in Table I (Section III) and considering the classical CHB-stage voltage balancing approach as in [9], an example is provided in Fig. 2 in case linear PI controllers adjust the CHB cells voltage. The results are related to different initial voltage conditions and it can be observed that the CHB-balancing, in the start-up procedure, can bring the system to a stable (Fig. 2a) or unstable (Fig. 2b) operation if the DC-link voltages are initially balanced or unbalanced. In Fig. 2a), the overall MV DC-link voltage control and the balancing control are turned on at t = 3s, while a 10% capacitor parameter mismatch occurs at t = 6s; in this case satisfactory performance is verified. In Fig. 2b), a 10% capacitor parameter mismatch is considered as initial condition involving unbalanced MV DC-link voltages.

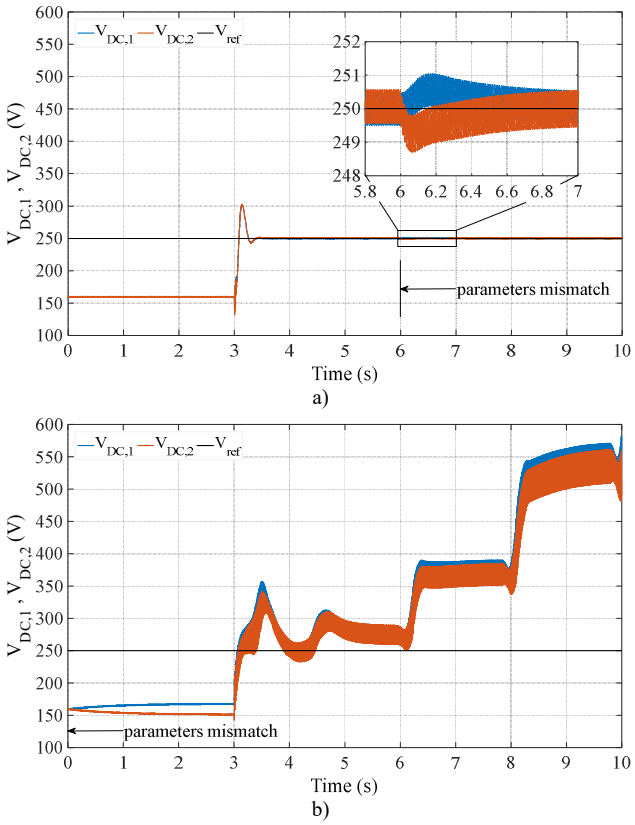

Fig. 2. CHB-stage voltage balancing in stable a) and unstable b) scenarios.

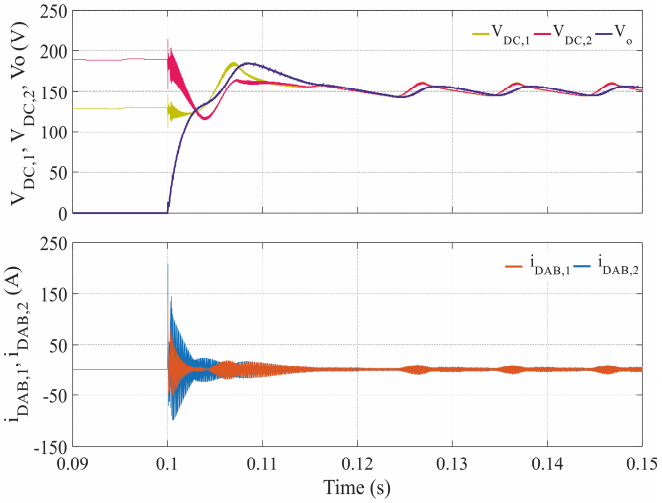

Fig. 3. Top: LV DC-link (V_o) and MV DC-link voltages ($V_{DC,1}$ and $V_{DC,2}$), Bottom: DABs inrush current during start-up without soft-charging procedure.

As a consequence, the same start-up procedure leads the system into unstable condition.

Superior ST start-up performance can be achieved in case the ST is controlled as a unique and full-interconnected system with the balancing strategy performed into the isolation stage [10]. This approach can avoid the risk of overvoltages or/and over-currents in the CHB converter. The DAB converters, with integrated voltage balance controllers, start before the CHB converter, and as a consequence balanced voltages of the DC-links in the MV side are achieved.

B. Soft-charging of the DC-link capacitor in the LV side

The pre-charging of the DC-link capacitor in the LV side is necessary as initial condition to start the control of the DAB converters, while an energized MV DC-link is connected to the input port of the DC/DC isolation stage. Indeed, at the DAB converters start-up, the uncharged capacitors would act as virtual short circuits allowing a fast increase of the current over the rated and safe operating conditions. At this stage, the DABs starting current is not determined by the controlled phase-shift angle between the voltages at the primary and secondary side of the HFT, but it is only determined by the electrical circuit parameters. Hence, the HFT peak current value is directly proportional to the equivalent input voltage.

Referring to the power stage parameters reported in Table I (Section III), in Fig. 3 there are shown the inrush currents in each HFT of the DABs ($i_{DAB,1}$ and $i_{DAB,2}$) when an energized MV DC-link ($V_{DC,1}$ and $V_{DC,2}$) is connected to the input port of the DABs and the LV DC-link capacitor is phase-shift controlled from a zero initial voltage V_o. To avoid this potentially harmful current, a soft-charging procedure of the LV capacitor starting from the energized MV side is proposed in [27] enabling inrush current limitation in the DAB converters start-up. In this paper it is hereby extended to the ST application.

C. Overall ST start-up scheme

The overall scheme of the proposed ST start-up procedure is shown in Fig. 4a): at first, the MV DC-link capacitors are charged with the CHB acting as a passive rectifier; later the LV

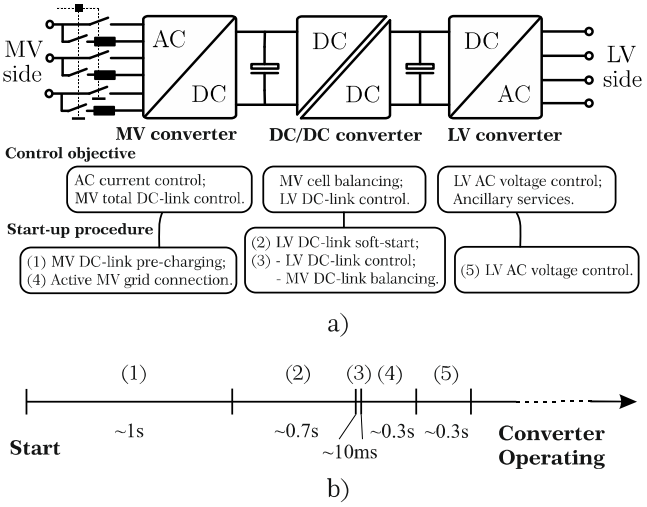

Fig. 4. Smart Transformer control and start-up procedure: a) control objective of each ST stage and b) start-up procedure timeline.

DC-link capacitor is charged through a modified modulation technique applied just to the primary H-Bridge of each DAB converter; successively the DAB converters are activated controlling both the LV DC-link voltage and the balance of the MV DC-links; finally, the CHB is activated to control the overall MV DC-link. In Fig. 4b) a timeline with the indicative duration of each step of the proposed start-up procedure is shown. The first two steps are the most time consuming due to the MV and LV DC-link capacitor pre-charging. Instead, the duration of the remaining steps mostly depends on the control bandwidth designed in each control loop.

III. ST Modeling And Balance Control

The design of the start-up procedure depends on the ST power stages topologies, their control systems and the operation modes. However, the ST can be controlled and soft-started as a unique converter.

In this case the small signal model of the ST as a full interconnected system is fundamental in order to tailor the control system design and to carry out a tuning procedure, taking into account voltages imbalance condition.

The model of the first two stages of the ST can be derived as in [10], referring to Fig. 5. The i-*th* cell small signal model of the CHB is represented by the following equations:

$$\tilde{V}_{DC,i} = \frac{\left(\bar{I}_g L_g s + N\bar{V}_{DC,i}\bar{M}\right)\tilde{I}_{g,i} - 2N\bar{V}_{DC,i}\tilde{I}_{DC,i}}{\left(2N\bar{V}_{DC,i}C_i s + N\bar{I}_g\bar{M}\right)} \tag{1}$$

$$\tilde{I}_{g,i} = \frac{N\bar{V}_{DC,i}\tilde{d}_i - E}{\left(L_g s + R_g\right)} \tag{2}$$

where L_g and R_g represent the grid impedance parameters, E is the grid voltage, $\bar{I}_g$ is the rated grid current amplitude, $\bar{M}$ is the rated modulating signal amplitude, N is the number of CHB cells, C_i is the i-*th* MV capacitance, $\bar{V}_{DC,i}$ is the i-*th* MV DC-link nominal value and d_i is the duty-cycle of the i-*th* CHB cell.

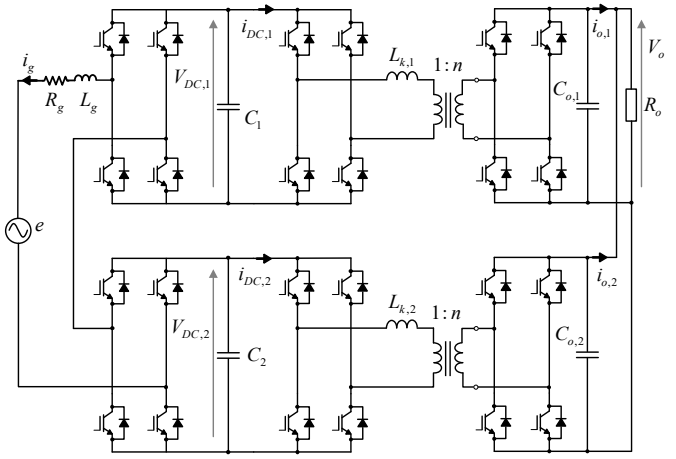

Fig. 5. ST with a 5-level CHB and output parallel DABs configuration.

The DAB converters are modeled in the input and output side as current sources [10], denoting the input current with $I_{DC,i}$ and the output current as $I_{o,i}$. The DAB small signal model is represented by the following equations:

$$\tilde{I}_{DC,i} = G_\varphi \tilde{\varphi}_i + G_V \tilde{V}_o \tag{3}$$

$$\tilde{I}_{o,i} = G_\varphi \tilde{\varphi}_i + G_V \tilde{V}_{DC,i} \tag{4}$$

where V_o is the LV-DC output voltage, φ_i is the phase shift of the i-*th* DAB and:

$$\begin{aligned} G_\varphi &= \frac{T_{DAB}}{2L_k n}\left(1 - 2\bar{\Phi}\right)\bar{V}_{DC} \\ G_V &= \frac{T_{DAB}}{2L_k n}\left(1 - \bar{\Phi}\right)\bar{\Phi} \end{aligned} \tag{5}$$

T_{DAB} is the DAB switching period, L_k is the equivalent inductance of the HFT, n is the HFT turn ratio and $\bar{\phi}$ is the steady-state DAB phase shift angle between the voltages at the primary and secondary side of the HFT. Assuming that the outputs of the DAB converters are parallel connected, the resulting output voltage is:

$$\tilde{V}_o = \frac{R_o}{R_o C_o s + 1}\sum_{i=1}^{N}\tilde{I}_{o,i} = \frac{R_o}{R_o C_o s + 1}\sum_{i=1}^{N}\left(G_\varphi\tilde{\varphi}_i + G_V\tilde{V}_{DC,i}\right) \tag{6}$$

where R_o and C_o are respectively the equivalent LV DC output resistance and capacitance, and N is the number of parallel DAB converters. In order to decouple the output voltage from the variations of each DC-link voltage, an additional term can be added to the phase shift of each DAB converter as shown in Fig. 6. The gray branch in Fig. 6 contributes to the output voltage control, thus it can be neglected in the balancing transfer function between the i-*th* DAB phase shift and the i-*th* DC-link voltage.

$$\tilde{\varphi}_i = -\tilde{\varphi}_i^* - \frac{G_V}{G_\varphi}\tilde{V}_{DC,i} \tag{7}$$

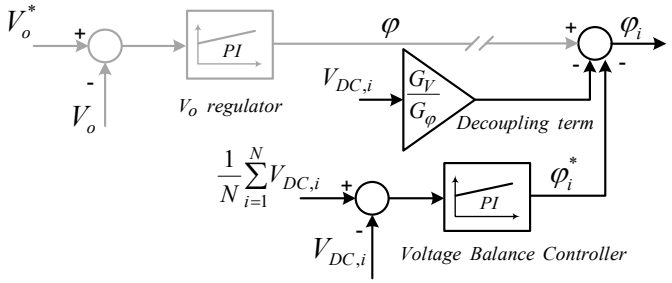

Fig. 6. Control scheme of the ST DC/DC power conversion stage.

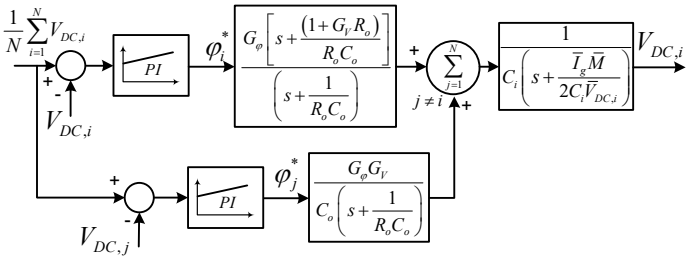

Fig. 7. Voltage balance control of the ST DC/DC power conversion stage.

Substituting (7) in (3), the DAB converter current can be expressed as:

$$\tilde{I}_{DC,i} = -G_\varphi \tilde{\varphi}_i^* + G_V \tilde{V}_o - G_V \tilde{V}_{DC,i} \tag{8}$$

The last term in (8) can be compensated modifying the duty-cycle of the i-*th* CHB cell as:

$$\tilde{d}_i = \tilde{d}_i^* - \frac{2G_V\left(L_g s + R_g\right)}{\left(\bar{I}_g L_g s + N\bar{V}_{DC,i}\bar{M}\right)}\tilde{V}_{DC,i} \tag{9}$$

In case of perfect compensation, the entire system can be described by a new set of equations as follows:

$$\tilde{I}_{o,i} = -G_\varphi \tilde{\varphi}_i^* \tag{10}$$

$$\tilde{I}_{DC,i} = -G_\varphi \tilde{\varphi}_i^* + G_V \tilde{V}_o \tag{11}$$

$$\tilde{V}_{DC,i} = \frac{\left(\bar{I}_g L_g s + N\bar{V}_{DC,i}\bar{M}\right)\tilde{I}_{g,i}^* - 2N\bar{V}_{DC,i}\tilde{I}_{DC,i}}{\left(2N\bar{V}_{DC,i}C_i s + N\bar{I}_g\bar{M}\right)} \tag{12}$$

$$\tilde{I}_{g,i}^* = \frac{N\bar{V}_{DC,i}\tilde{d}_i^* - E}{\left(L_g s + R_g\right)} \tag{13}$$

Substituting (10) and (6) in (11), it results:

$$\tilde{I}_{DC,i} = -\tilde{I}_{o,i} - G_V\left(\frac{R_o}{R_o C_o s + 1}\right)\sum_{j=1}^{N}\tilde{I}_{o,j} \tag{14}$$

$$\tilde{I}_{DC,i} = -\frac{G_\varphi\left(R_o C_o s + 1 + G_V R_o\right)}{\left(R_o C_o s + 1\right)}\tilde{\varphi}_i^* - \left(\frac{G_\varphi G_V R_o}{R_o C_o s + 1}\right)\sum_{\substack{j=1\\ j\neq i}}^{N}\tilde{\varphi}_j^* \tag{15}$$

Limiting the analysis to the effects of the phase shift variation on the voltage balance, the term with $I_{g,i}$ in (12) can be neglected. Substituting (15) in (12), it results in:

$$\tilde{V}_{DC,i} = \frac{G_\varphi\left(s + \frac{1+G_V R_o}{R_o C_o}\right)\tilde{\varphi}_i^* + \frac{G_\varphi G_V}{C_o}\sum_{\substack{j=1\\ j\neq i}}^{N}\tilde{\varphi}_j^*}{C_i\left(s + \frac{\bar{I}_g\bar{M}}{2C_i\bar{V}_{DC,i}}\right)\left(s + \frac{1}{R_o C_o}\right)} \tag{16}$$

Choosing a PI for the balance control (Fig. 7), it results:

$$\tilde{\varphi}_i^* = K_{BAL,i}\left(\frac{s + K_{I,i}}{s}\right)\left(\frac{1}{N}\sum_{i=1}^{N}\tilde{V}_{DC,i} - \tilde{V}_{DC,i}\right) \tag{17}$$

where $K_{BAL,i}$ denotes the proportional gain and $K_{I,i}$ denotes the integral gain. The integral gain can be set in order to delete the slowest pole, hence it can be defined as:

$$K_{I,i} = \frac{\bar{I}_g\bar{M}}{2C_i\bar{V}_{DC,i}} \tag{18}$$

$K_{BAL,i}$ can be tuned on the basis of the desired bandwidth and phase margin of the voltage balance open loop transfer function G_{BAL}. The overall open loop transfer function G_{BAL} can be defined as:

$$G_{BAL}(s) = \frac{\frac{1}{N}\sum_{i=1}^{N}\tilde{V}_{DC,i}}{\tilde{V}_{DC,i}} = \frac{K_{BAL,i}G_\varphi\left(s + \frac{1+NG_V R_o}{R_o C_o}\right)}{C_i s}\frac{N(s)}{D(s)} \tag{19}$$

with *N(s)* and *D(s)* defined as:

$$N(s) = 1 + \frac{\frac{K_{BAL,i}G_\varphi}{C_i}\left(s + \frac{1+G_V R_o}{R_o C_o} - \frac{G_V}{C_o}\right)}{s\left(s + \frac{1}{R_o C_o}\right)} = \frac{s + \frac{K_{BAL,i}G_\varphi}{C_i}}{s} \tag{20}$$

$$D(s) = \frac{\left(s + \frac{1}{R_o C_o}\right)\left(s + \frac{K_{BAL,i}G_\varphi}{C_i}\right) + (N-1)\frac{K_{BAL,i}G_\varphi}{C_i}\frac{G_V}{C_o}}{s\left(s + \frac{1}{R_o C_o}\right)} \tag{21}$$

Denoting the following constant gains as:

$$K_{sys} = \frac{K_{BAL,i}G_\varphi}{C_i} \qquad T_o = R_o C_o \qquad Q = \frac{G_V}{C_o} \tag{22}$$

The open loop transfer function becomes:

$$G_{BAL}(s) = \frac{K_{sys}\left(s + \frac{1}{T_o} + NQ\right)\left(s + K_{sys}\right)}{s\left[\left(s + \frac{1}{T_o}\right)\left(s + K_{sys}\right) + (N-1)QK_{sys}\right]} \tag{23}$$

Considering a ST based on a 5-level CHB converter and two DAB converters with the power stage parameters defined in Table I, the Bode diagram of the voltage balance transfer function G_{BAL} is represented in Fig. 8. Neglecting the small deviation in the low frequency area, it can be approximated to the Bode diagram of an integrator with gain equal to K_{sys}. The computational delay is taken into account with a first order transfer function whose time constant is equal to the switching period of the DAB, T_{DAB}.

As defined in (22), the gain of the system is proportionally dependent on the value of K_{BAL}. The Bode diagram of the voltage balance loop transfer function G_{BAL} is shown for different values of K_{BAL} in order to provide a tuning guide line, based on the desired bandwidth. Looking at Fig. 8, the bandwidth of the voltage balance loop (about 50 Hz) is chosen in order to be about ten times smaller than the bandwidth of the output voltage control loop. In conclusion, the small-signal model of the ST is required for the tuning of the voltage balancing controller achieving decoupling between the output voltage control loop and the voltage balancing control loop.

Considering the tuning strategy presented in [10] and the controller parameters in Table I, in Fig. 9, the dynamic response of the DABs output voltage control loop at different reference signals is shown. Firstly, the response of the system to a reference voltage step ΔV_o*=10V (R_o = 32Ω) is shown at t=1s in case of 10ms settling time. It can be observed that the controller parameters are chosen in order to guarantee that the output voltage control loop is at least ten time faster than the CHB voltage control loop. Secondly, at t = 1.1s, the input voltage V_{DC} has been imposed as output voltage reference (V_o*=V_{DC}) and a ramp voltage with a slop of 80V/80ms (1kV/s) is set as reference. Hence the voltage reference raises from 170V to 250V in order to emulate the start-up procedure. The results prove tracking capability with settling time of 120ms and negligible overshoot (around 0.2V). Instant power transfer between the MV and LV DC-links matches limited peak current in the DABs HFTs. The peak current in the HFT depends on the difference between the input and output voltage.

TABLE I
POWER STAGE AND CONTROL PARAMETERS

Symbol	Description	Value
e	Grid Voltage (RMS)	230 *V*, 50 *Hz*
L_g	Filter Inductance (MV side)	3.8 *mH*
$V_{DC,1}$=$V_{DC,2}$	Rated MV DC-link voltage	250 *V*
V_o	Rated LV DC-link voltage	250 *V*
C_1, C_2	MV capacitance	930 *μF*, 920 *μF*
C_o	LV capacitance	920 *μF*
R_o	Rated, light load resistance	32 *Ω*, 10 *kΩ*
$L_{k,1}$, $L_{k,2}$	Leakage inductance HFT	33 *μH*, 30 *μH*
$R_{p,1}$, $R_{p,2}$	DC-link parallel resistance	9 *kΩ*, 10 *kΩ*
n	HFT turn ratio	1
$f_{sw,CHB}$	CHB switching frequency	3 *kHz*
$f_{sw,DAB}$	DAB switching frequency	12 *kHz*
P_n	ST nominal power	2 *kW*
DP25H1200T1016	IGBT module	*1200V, 25A*$_{RMS}$
$K_{p,cc}$	MV current proportional gain	*10*
$K_{res,cc}$	MV current resonant gain	*1000*
$K_{p,MVdc}$	MV DC-link proportional gain	*0.04*
$K_{i,MVdc}$	MV DC-link integral gain	50
$K_{p,LVdc}$	LV DC-Link proportional gain	0.001
$K_{i,LVdc}$	LV DC-Link integral gain	50
$K_{p,bal}$	MV balancing proportional gain	0.0025
$K_{i,bal}$	MV balancing integral gain	30

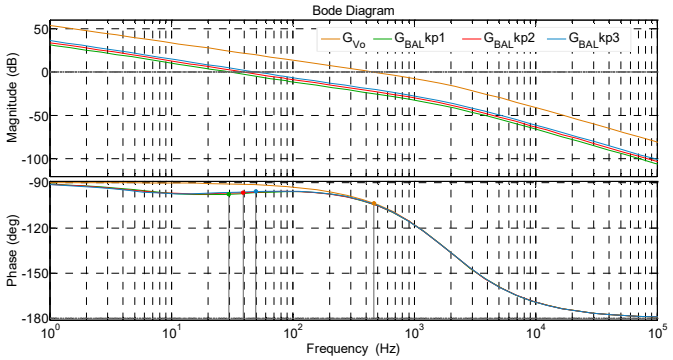

Fig. 8. Bode diagram of the voltage balance open loop transfer at different values of $K_{BAL,i}$.

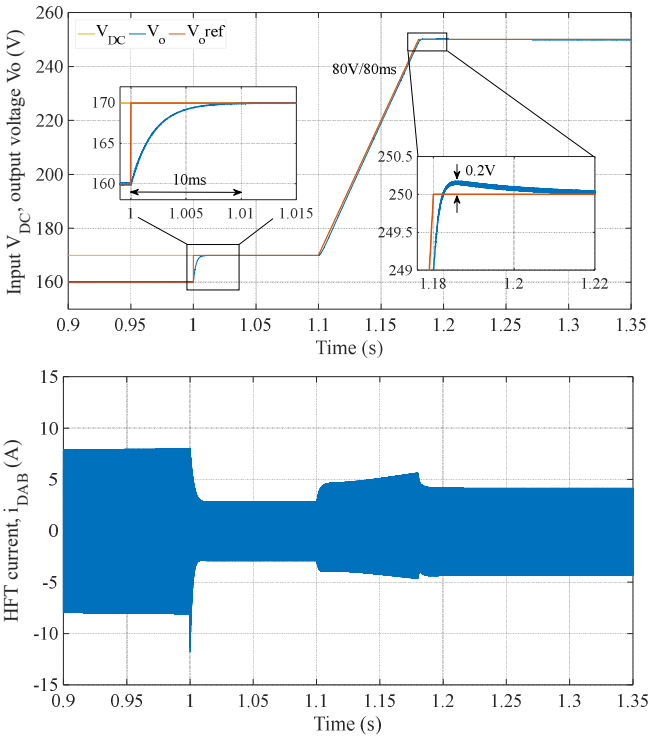

Fig. 9. Top: DAB output (V_o) and MV input voltage (V_{DC}), Bottom: DAB HFT primary side current during a dynamic response test at different reference signals, step signal at t=1s and 1kV/s slope ramp signal at t=1.1s.

IV. ST: SOFT-START PROCEDURE

The proposed soft start procedure deals with the three-stage ST whose model and control systems are analyzed in Section II. It consists of four steps described in the following and providing as advantages: balanced DC-link voltages in the ST MV side and inrush current limitation.

A. First step

The first step consists in the connection of the CHB converter to the main grid. The system is charged through a pre-charging resistor connected between the grid and the AC side of the AC/DC converter in order to avoid a large inrush current. The resistor is then by-passed meanwhile passive rectifier operation is perpetuated by the anti-parallel freewheeling diodes of the CHB converter to charge the MV DC-link capacitors.

In this condition, no loads are connected to the DC-links in the MV side. The power drained from the main grid is limited to the amount required to supply the MV DC-link capacitors C_i,

internal series resistance $R_{s,i}$ and the parallel resistance $R_{p,i}$. The parallel resistances do not absorb significant power compared to the rated power of the ST since $R_{p,i}$ are in the kΩ range. In Fig. 10 the components involved in the current path are marked in black, whereas the devices in gray are turned off.

Due to the mismatch of the capacitances and resistances parameters (see Table I), the steady-state voltage values in the DC-links are different: $V_{DC,1} \neq V_{DC,2}$. At no load operation, the effect of the parameters mismatch is amplified and the voltages are significantly unbalanced.

B. *Second step*

The aim of the next steps is to overcome the voltage imbalance, which results from the first step, through a balancing procedure operated by the DAB converters. A similar approach has been proposed in [19] avoiding the occurrence of overcurrent during the turn-ON of the DAB converters and in case of no pre-charging of the output capacitor $C_{o,i}$.

The phase-shift angle between the primary and secondary voltages of the HFT cannot be used to reduce the inrush current. Differently, the maximum inrush current can be adequately reduced by controlling the zero-voltage state in the leading bridge of the DAB. In this paper the zero-voltage-state is obtained applying an independent switching law to the two legs of the same H-Bridge. In particular, the zero-voltage-state is achieved shifting the carrier of the leg B with respect to the carrier of the leg A. In such way, when in a switching period T_{DAB}, both S_1 and S_3 are turned ON or OFF, the voltage in the primary side of the HFT is zero.

In Fig. 11 the switching signals, related to the first bridge of the DAB converter, are represented in four different shift cases with the related primary and secondary voltages, and the current in the HFT. For each DAB, when the first bridge of the DAB is turned on, the second bridge is kept off. The switches in the primary side are driven as in Fig. 11, varying the time shift from zero to $T_{DAB}/2$ with a ramp signal. This modulation can be denoted as DAB soft-shift start modulation (SSSM).

Due to the discontinuous conduction mode, the current through the transformer leakage inductance appears limited avoiding the burnout of the IGBTs. During this second step, the second bridge of the DAB operates as a diode rectifier (Fig. 12). The transferred power pre-charges the output capacitor up to a

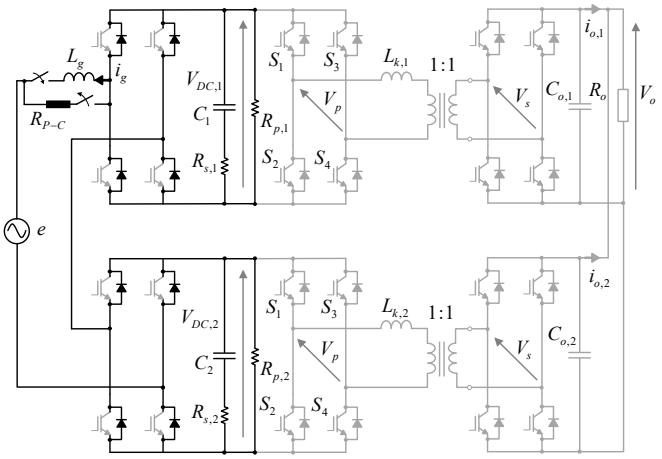

Fig. 10. ST with a 5-level CHB during MV side capacitor pre-charging.

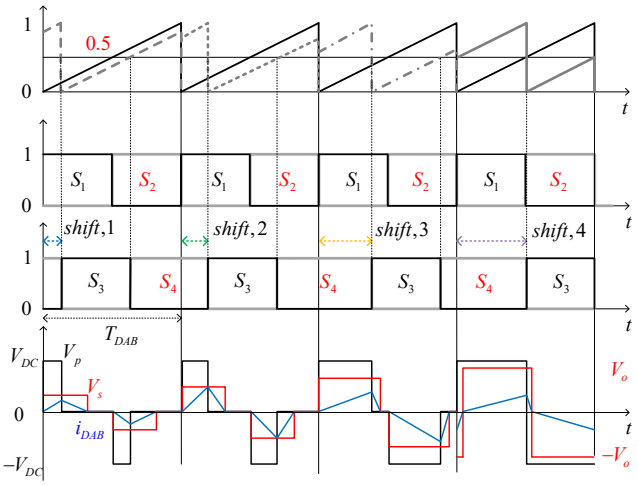

Fig. 11. DAB HFT quantities and gate driver signals during the shift start.

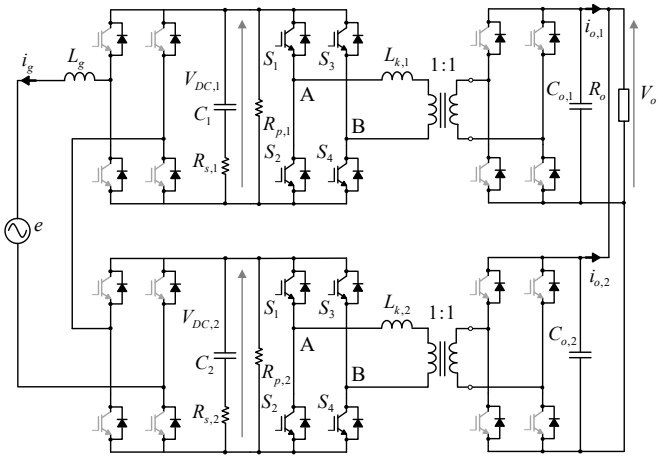

Fig. 12. ST during the second step of the soft-start procedure.

voltage value which depends on the input voltage value, on the voltage drops across the semiconductors devices and on the transformer internal resistance.

The pre-charging voltage induces current circulation into the load and a certain amount of power flows from the grid to the DC load. The CHB converter in the second step still operates as a passive rectifier, and as a consequence the grid current is highly distorted. The grid current increases slowly and it avoids overcurrent also in the CHB converter. Also the output voltage and leakage inductance current increase slowly. The velocity of the pre-charging procedure depends on the slope of the ramp used to increase the time shift between the two carrier signals of the first H-Bridge in each DAB converter. The second result of this step is the convergence of the DC-link voltages to a new steady-state point characterized by a smaller voltage imbalance than the previous state (see Fig. 13 at $t_1 = 0.4$s where the system is in *no-load* operation and R_o is connected but not energized).

Considering the power stage parameters reported in Table I (with $R_o = 32\Omega$), the voltages and current waveforms are shown in Fig. 13-14 in the time interval between $t_2 = 0.5$s and $t_3 = 1$s. The new reached steady-state leads to the next step. In Fig. 15, the HFT primary side currents during the soft-start procedure are shown. Considering the IGBTs module rating (Table I), the current in each DAB is inside the safe operating area.

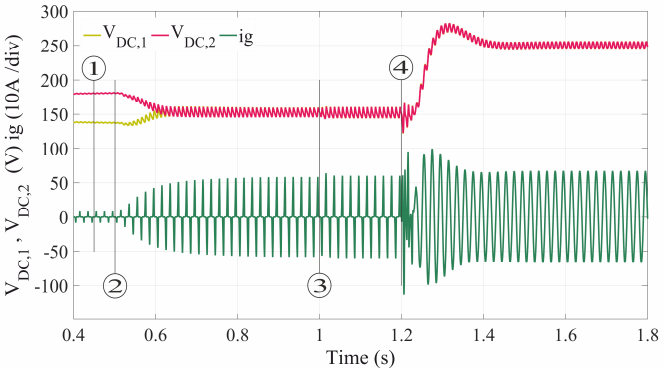

Fig. 13. $V_{DC,1}$ and $V_{DC,2}$, grid current ig during the soft-start procedure at rated load operation (simulation).

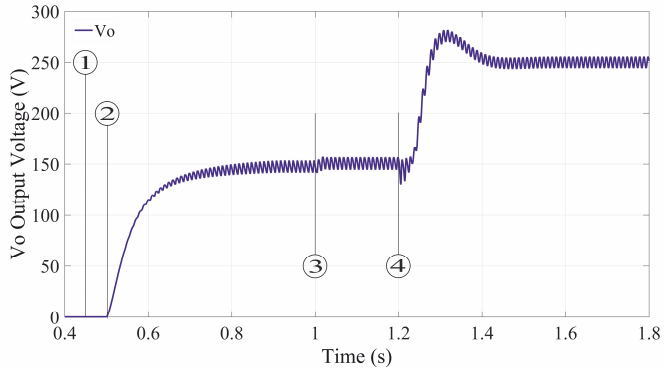

Fig. 14. DABs output voltage V_o during the soft-start procedure at rated load operation (simulation).

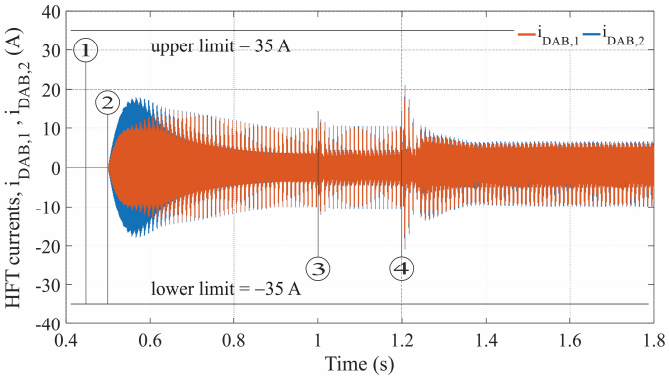

Fig. 15. DABs HFT primary side currents during the soft-start procedure at rated load operation (simulation).

B.1 Soft-switching of the DAB soft-charging procedure

Soft-switching operation is verified in the primary H-Bridge of each DAB during the LV soft-charging procedure. The soft-switching analysis is provided for the primary side H-Bridge since the secondary side is not controlled (diode rectifier). To analyze the soft-switching capability, the typical DAB HFT voltages, current and gate driver signals during the soft-charging in discontinuous conduction mode (DCM) are shown in Fig. 16.

Here, V_P, V_S and i_{DAB} indicate respectively the primary and secondary side voltages and the current in the DAB HFT. ZCS and ZVS indicate zero-current and zero-voltage soft-switching conditions. From Fig. 16 it can be seen that ZCS occurs at the turn-OFF of S_2 and consequently at the turn-ON of S_1, due to the zero current shown at the switching condition.

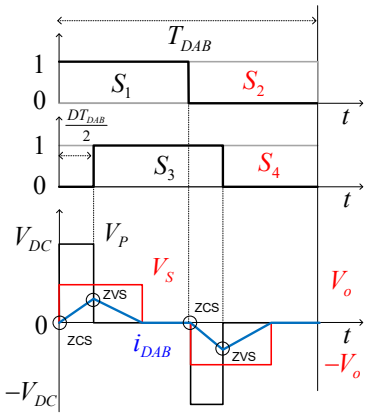

Fig. 16. Switches gate driver signals, V_P, V_S, and i_{DAB} of the DAB converter.

On the other way around, ZCS occurs at the turn-OFF of S_1 and consequently at the turn-ON of S_2. Analyzing S_3 and S_4, ZVS occurs at the turn-ON in both S_3 and S_4, while hard-switching (HS) occurs at the turning-OFF in both S_3 and S_4. Soft-switching is verified in the following cases: S_1 and S_2 have ZCS at turn-ON/OFF, S_2 and S_4 have ZVS at turn-ON.

B.2 Design of the ramp slope-rate for the DAB soft-start

The design of the ramp slope-rate used in the DAB soft-start procedure is based on mathematical calculation of the DAB HFT current peak.

Looking at Fig. 16, $(DT_{DAB})/2$ denotes the generic time-shift as a function of the duty-cycle D (with $0 \le D \le 1$). In a switching period T_{DAB}, $(DT_{DAB})/2$ represents respectively the time duration of the positive and negative voltage related to the overall V_P waveform.

Considering a constantly energized MV DC-link with $V_{DC,i}$ as input voltage and assuming the output voltage V_o constant for a period, the current in the DAB HFT increases with a fixed rate. In a switching period the current peak value related to the primary side HFT is:

$$I_{DAB,pk}\Big|_{T_{DAB}} = \frac{\left(\hat{V}_P - \hat{V}_S\right) DT_{DAB}}{2L_k} = \frac{\left(V_{DC,i} - V_o\right) DT_{DAB}}{2L_k} \qquad (24)$$

Thus, (24) gives evidence that the peak value of the HFT current in the primary side depends on the difference between the MV and LV DC side voltage, and it depends on the value of the duty-cycle in that period. The switches in the primary side are driven varying the time shift $(DT_{DAB})/2$ from zero to $T_{DAB}/2$ with a ramp signal or, equivalently, varying the duty-cycle from zero to 1. As a result, the output voltage V_o rises up to the steady-state value with a trend that can be reasonably approximated to a linear function as follows:

$$\begin{aligned} D(t) &= r_d\, t \qquad 0 \le D \le 1 \\ V_o(t) &\approx r_o\, t \qquad 0 \le V_o \le V_{DC,i} \end{aligned} \qquad (25)$$

where r_d (s^{-1}) and r_o (V/s) are the slope-rate of the duty-cycle D and of the output voltage V_o, respectively. By substituting (25) in (24), the resulting function, which represents the time

evolution of the HFT current peak during the soft-charging process, can be expressed by:

$$i_{DAB,pk}(t) \approx \frac{T_{DAB}\, r_d}{2L_k}\left[V_{DC,i}\, t - r_o\, t^2\right] \tag{26}$$

$$I_{DAB,pk} = i_{DAB,pk}(t)\Big|_{t=\frac{V_{DC,i}}{2r_o}} \tag{27}$$

where (26) represents the equation of a parabola, while $I_{DAB,pk}$ is the maximum value assumed by the peak current during the soft-charging process. More generically, (26) can be written as

$$r_o = f(r_d) \Rightarrow i_{DAB,pk}(t) \approx \frac{T_{DAB}\, r_d}{2L_k}\left[V_{DC,i}\, t - f(r_d)\, t^2\right] \tag{28}$$

where it is highlighted that the output voltage slope-rate is a function of the duty-cycle slope-rate.

Eq. (26) - (28) are validated by simulation results conducted during the soft-charging for different values of r_d, as shown in Fig. 17. The parameters can be derived from Table I, when light-load condition is applied and $V_{DC,i}$ = 250V. Similar results would be found in case of soft-charging at rated load condition, but they are not included in the paper.

Simulation results show that each current in the primary side of HFT is enveloped by the parabolic current as obtained by (28). Furthermore, the maximum inrush current peak $I_{DAB,pk}$ calculated by (27) matches exactly with the peak value provided by the simulation.

Differently in Fig. 18 there are reported the values of the HFT inrush current peaks for different values of the duty-cycle slope-rate r_d and for different values of the input voltage $V_{DC,i}$. The results show that the higher is r_d, the faster is the charging process, at the expense of higher HFT inrush current peaks.

Furthermore, Fig. 18 demonstrates that it is possible to accelerate the charging process duration in low input voltage $V_{DC,i}$ condition. As a consequence the DAB can be soft-started and controlled ensuring high performance operation also before the CHB MV DC-link reaches the rated voltage value.

In conclusions the duty-cycle slope can be derived from the previous equations and/or from graphical representation as shown in Fig. 18 and Fig. 19 considering the power modules maximum peak current, the input voltage $V_{DC,i}$ and the start-up time constraint.

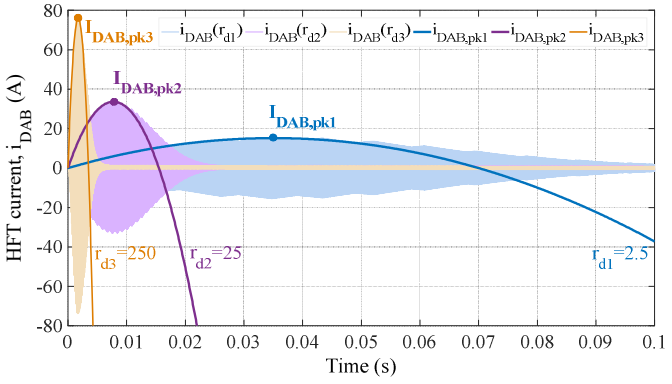

Fig. 17. HFT DAB current compared to the current estimated by (26) or (28) at several duty-cycle slope-rate, $V_{DC,i}$ = 250V, at light-load operation.

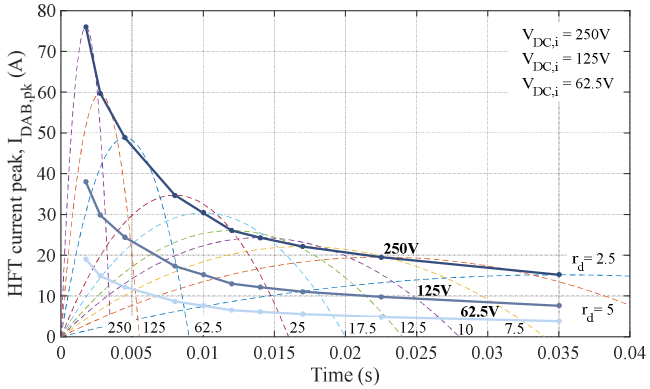

Fig. 18. HFT inrush current peak estimated by (26) or (28) for several duty-cycle slope-rates r_d and input voltages $V_{DC,i}$, at light-load operation.

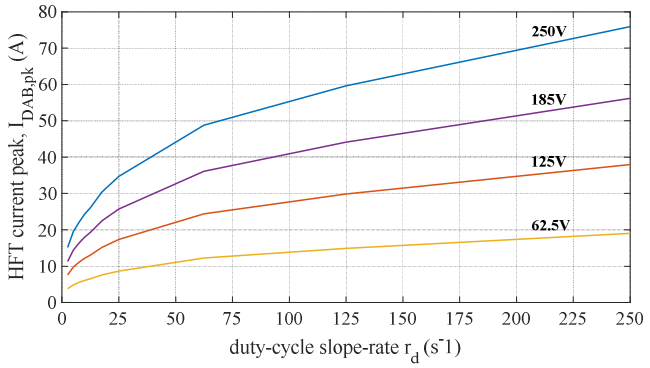

Fig. 19. HFT inrush current peaks as function of the duty-cycle slope-rate for several input voltages $V_{DC,i}$, at light-load operation.

C. *Third step*

Due to the voltage drop across the devices of the first H-Bridge, across the HFT and across the freewheeling diodes of the second H-Bridges, the DAB converters output voltage value is lower than the input rectified voltage. In order to compensate this voltage drop, a proper control action of the output voltage is required. Turning on the switches in the second DAB H-bridge and adjusting properly the value of φ_i (phase shift control variable), the control of V_o can be achieved. Hence, the reference is varied up to V_o^*, which can be set as:

$$V_o^* = \sum_{i=1}^{N} \frac{V_{DC,i}}{N} \tag{29}$$

At the same time also the voltage balance control is turned on. The balancing is performed by the DAB converters adjusting properly the phase shift, φ_i. At the end of the third step, the following conditions are verified: the DC-link voltages are perfectly balanced by the DAB balance controllers and the output voltage V_o is controlled through a PI controller (control scheme of Fig. 6). This third step is summarized in Fig. 13-15 in the time interval between t_3 = 1s and t_4 = 1.2s.

D. *Fourth step*

In this stage, the CHB converter switches from passive rectifier to active rectifier operation and the total MV voltage control can be achieved. The parameters of the CHB voltage controller are set in order to achieve a trade-off between fast dynamics and low overshoot (Fig. 13).

The DABs controller parameters are tuned in order to guarantee dynamic performance around ten times faster than the CHB voltage controller [10]. The CHB control parameters are reported in Table I.

At the beginning of the fourth step, the output voltage reference V_o^* is set as in (29) and the secondary bridges behave similarly to the primary bridges for each DAB converter. The voltage balance is verified during all the transient behavior and dangerous overvoltages and/or over currents are avoided. Since the DAB controller exhibits fast dynamic performance and full voltage control, the DC/DC isolation stage guarantees fast power transfer between the MV and LV AC side. When the nominal steady-state MV DC-link voltage is reached, the output voltage reference V_o^* is set to its nominal value. The MV DC-link voltages and the grid current are represented in Fig. 13 in the time interval between t_4 = 1.2s and t_5 = 1.8s. The output voltage V_o is represented in Fig. 14.

E. Fifth step

The proposed ST is based on a three-stage architecture, however the focus of the paper is on the start-up of the first two stages. As in [10], the proposed architecture is conceived to be coupled with DC smart grids. For this reason it has to be considered also the event that the LV DC-link is directly connected to DC loads, sources or distribution bus. In order to avoid loss of generality, some hints about the start-up procedure of the DC/AC converter in a ST-fed grid are here given.

The LV side converter is in charge of forming the grid. The main requirement to take into account during the first grid energization is the necessity to avoid instabilities which can arise in several points of the grid due to different loads properties and configurations. In [8] an innovative procedure based on online grid identification and lead-element filtering is proposed to energize the grid and to connect step by step each loads when stable grid condition is verified.

During the ST-fed grid startup, the power is firstly used to energize feeders with a majority of passive loads. The ST LV side voltage will not reach the nominal value but a low value so that all the grid-converter-based DERs cannot connect to the grid. The grid voltage will increase gradually to the nominal value meanwhile an online grid impedance identification provides initial parameters to an adaptive stabilizing filter. Distributed sources and active loads including grid-converter-based DERs will connect to the grid when it is stable.

F. Soft-start procedure at light-load operation

The proposed start-up procedure is applied in a different power condition and in particular, when light-load operation persists during all the soft-start period. This condition is emulated in the model of the overall system with an output load R_o of 10kΩ. Fig. 20–21 show the DC-link voltages, the grid current and the output voltage during the soft-start procedure at light-load operation. In the first step condition, it is verified the same voltage imbalance of the previous case. Differently, when light-load condition is verified throughout all the start-up phases, the DC-link voltages remain unbalanced until the DAB output voltage and the DC-link balance controls are turned on.

The second step is presented in Fig. 20-21 in the time interval between $t_{2,\text{light-load}}$ = 0.1s and $t_{3,\text{light-load}}$ = 1s.

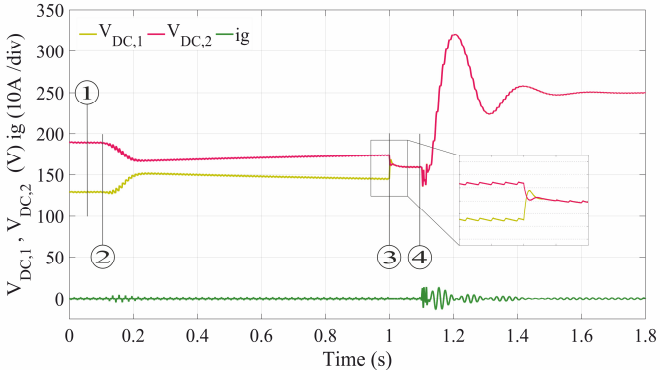

Fig. 20. $V_{DC,1}$ and $V_{DC,2}$, grid current (i_g) during soft-start procedure at light-load operation (simulation).

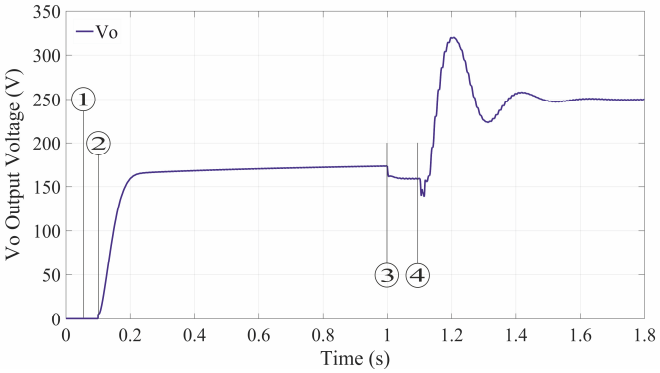

Fig. 21. V_o, DABs output voltage during soft-start procedure at light-load operation (simulation).

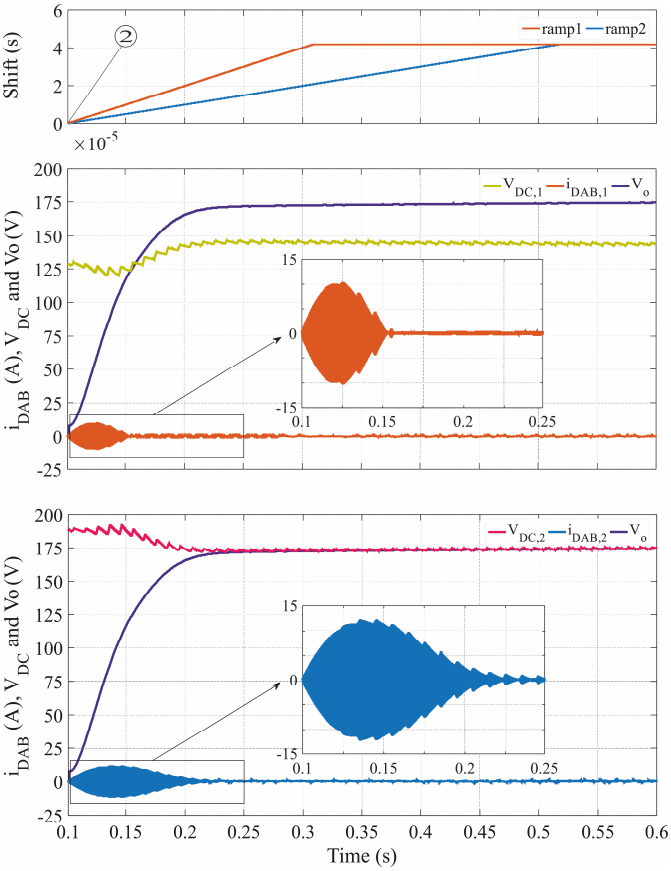

Fig. 22. DAB input voltage ($V_{DC,i}$), HFT primary side current ($i_{DAB,i}$) and DABs output voltage (V_o) during DABs soft-shift start at light-load operation.

In the start-up procedure previously described, the second step aims to the DAB converters inrush current limitation. During light-load operation, even small parameters mismatch between different power cells leads to great imbalance condition in the MV DC-link voltages, and consequently to unbalanced inrush current in each DAB converter.

The maximum inrush current can be equally shared by the DAB converters changing properly the slope of the soft-shift start ramp of each converter as shown in Fig. 22. Since the ramp slope depends on the difference between the input and output voltages, less slope corresponds to higher voltage difference. In Fig. 22 there are also shown the DABs input voltage $V_{DC,i}$, the HFT primary side-current $i_{DAB,i}$ and the output voltage V_o. In the same figure, a zoom in the HFT currents highlights the capability to share and to limit equally the maximum inrush current in both the DAB converters.

The last start-up procedure steps are performed in the time interval between $t_{3,\text{light-load}} = 1\text{s}$ and $t_{4,\text{light-load}} = 1.1\text{s}$ (Fig. 20-21) when the output voltage control and the DC-link balancing are activated, and between $t_{4,\text{light-load}} = 1.1\text{s}$ and $t_{5,\text{light-load}} = 1.8\text{s}$, when the CHB moves from passive to active rectifier operation.

V. Experimental Results

In order to validate the proposed soft-start procedure, a small scale ST prototype has been developed and shown in Fig. 23. It consists of a 5-level CHB active rectifier connected to the grid and DABs connected to each of the MV DC-links. For a proof of concept, the small scale ST prototype has been connected to a 230V/50Hz AC grid and each cell of the CHB converter contributes with 250V and the overall MV DC-link voltage is 500V. Without loss of generality, the acronym MV DC-link is here used referring to the DC-link connected to higher voltage side of the ST.

The DABs are parallel output connected and they feed a 2 kW resistive load. All H-bridges in the CHB converter and the DABs have been assembled with the same IGBT Danfoss module DP25H1200T101616 and the system is controlled with a dSPACE SCALEXIO system based on three DS2655 FPGA base boards; each board has been programmed with a FPGA Xilinx blockset toolbox. Each step of the start-up procedure has been experimentally proven and analyzed in detail. Looking at Fig. 23, the ST setup is depicted during control test in case of steady-state operation and unitary power factor operation.

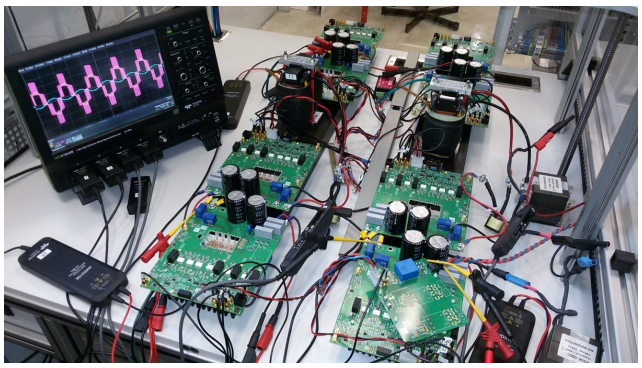

Fig. 23. ST setup: CHB and DAB converters control under test.

In Fig. 24 the MV DC-links voltages ($V_{DC,1}$, $V_{DC,2}$) and the grid current during the initial charge of the capacitors through the inrush resistor in the MV AC side are represented. The system is charged through a pre-charging resistor and the inrush peak current is minimized to a value of $6A_{peak}$.

In Fig. 25, the same quantities shown before are represented during the entire procedure period, with a zoom during the operation from passive to active rectifier. At the beginning of Fig. 25, the first step operation can be recognized; indeed, the ST is connected to the grid as a pure rectifier and, due to the parameter mismatches between the cells, the steady-state voltages reached in the MV DC-links are different.

Fig. 24. DC-link voltages $V_{DC,1}$ (yellow), $V_{DC,2}$ (red) and grid current i_g (green) with a zoom on the minimized inrush current during the MV AC side grid connection.

Fig. 25. DC-link voltages $V_{DC,1}$ (yellow), $V_{DC,2}$ (red) and grid current i_g (green) with a zoom during passive to active rectifier operation.

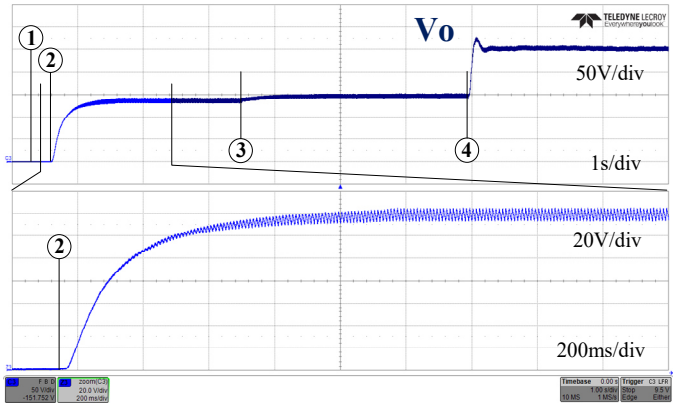

Fig. 26. Output voltage V_o during the start-up with a zoom on the second step.

The second step is represented by the pre-charging of the output voltage capacitors through the use of the DAB converters soft-shift start modulation. The second step results in convergence of $V_{DC,1}$ and $V_{DC,2}$ to a new steady-state point and it produces an increment of the absorbed grid current. In this new load condition, the parameter mismatch between the power modules corresponds with smaller voltage imbalance in comparison with previous step where the system was in *no-load* operation (R_o connected but not energized). The duration of the pre-charging depends on the DABs and the HFT rated current.

The duration of the pre-charging can be adjusted varying the slope of the ramp used to increase the time shift in the switching commands of the DAB legs.

In Fig. 26, the output voltage V_o during the entire procedure period is represented with particular focus to the pre-charging phase. During this phase, the output voltage rises with an over-dumped transient behavior similarly to a first order system and with an estimated duration of $T_{settling}$ = 1s. It represents a good trade-off between over-currents avoidance and a fast soft-start operation.

In Fig. 27, the primary and secondary side voltages of the HFT are represented together with the HFT primary side-current for three different values of the time shift during the soft-shift start pre-charging operation of the output voltage.

The fourth step is represented in Fig. 25 with a zoom during the transition from passive to active rectifier operation of the CHB converter. In this step the full control of the overall MV DC-link voltage is achieved. Meanwhile, the DAB converters control the output voltage V_o and the balance of the MV DC-links.

The output voltage reference is set to be equal to the instantaneous average value of the measured MV DC-link voltages as in (29). Due to the high bandwidth of the DAB converters control, it is possible for the DC/DC isolation stage to track and balance instantly the input MV DC-link voltages. Hence the DAB converters provides a fast power link transfer between the MV and LV AC side. The output voltage V_o during the third and the last stage is represented in Fig. 28. Remarkably, the experimental results fit the simulation results shown in Fig. 13 and Fig. 14, during all the soft-start operations and it proves the validity of the proposed structure.

TABLE II
PROPOSED START-UP VS STATE OF THE ART

Ref.	MV DC-link Balancing	Parameter Mismatch Tolerance	Without APU	DC/DC Inrush Current Control	Dynamic Analysis
[12]	✗	✗	✓	✓	✗
[13]	NQ	✗	✗	✗	✗
[14]	NQ	✗	✓	✗	✗
[15]	NQ	✗	✓	✓	✗
[17]	✗	✗	✗	✓	✗
[18]	✗	✗	✗	✗	✗
[19]	✓	✓	✓	✗	✗
[20]	✗	✗	✓	✓	✓
Our	✓	✓	✓	✓	✓

*NQ means Not Qualified for the comparison

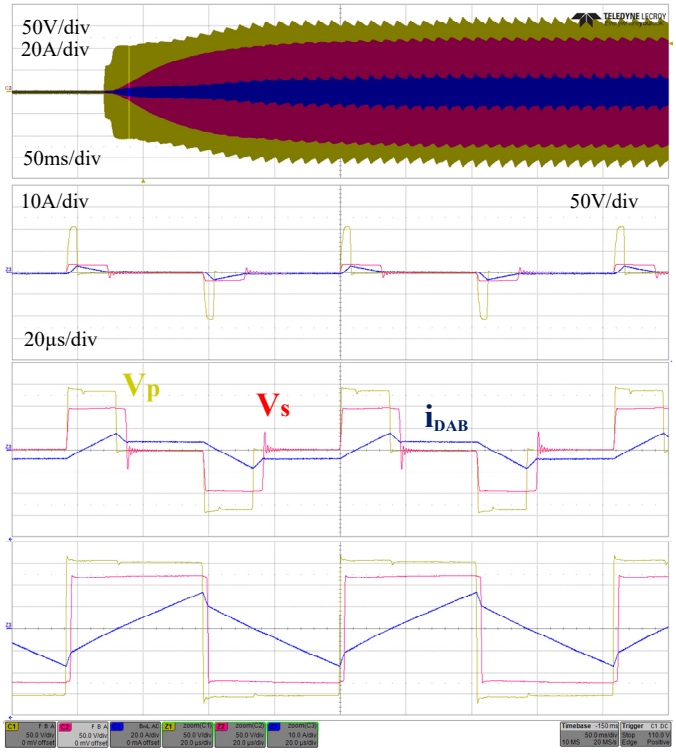

Fig. 27. HFT Primary (yellow) and secondary (red) side voltages, HFT primary side-current (blue) during the soft-shift start procedure.

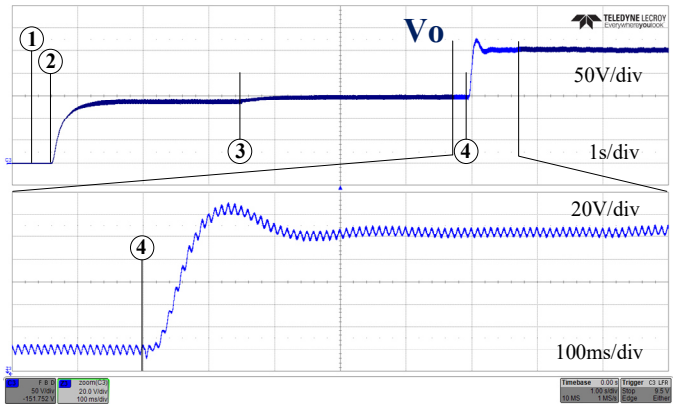

Fig. 28. Output voltage V_o during the start-up with a zoom on the transient from passive to active rectifier operation of the CHB converter.

VI. CONCLUSION

In this paper it is proposed a novel soft-start procedure designed for a three-stage ST based on CHB and DAB converters which is controlled as a unique converter. During the first steps of the start-up the CHB converter operates as a passive rectifier while the DC/DC power conversion stage adjusts the DC links capacitors voltages progressively to the reference value. The proposed SSSM modulation applied to the DAB converters allows to limit the inrush current avoiding overcurrent overshoots without the use of any APU. The adopted voltage control strategy ensures voltage balancing in every operation condition. Experimental results confirm the excellent performance of the proposed start-up procedure.

Final remarks are summarized in Table II, where the proposed start-up procedure is compared with the state of the

art in terms of MV DC-link balancing capability, parameter mismatch tolerance, inrush current controllability in each DC/DC converters, start-up dynamic analysis and absence of APUs.

REFERENCES

[1] "LV ENGINE" https://www.spenergynetworks.co.uk/pages/lv_engine.aspx.

[2] Q. Zhu, L. Wang, A. Q. Huang, K. Booth and L. Zhang, "7.2-kV Single-Stage Solid-State Transformer Based on the Current-Fed Series Resonant Converter and 15-kV SiCmosfets," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1099-1112, Feb. 2019.

[3] M. Leibl, G. Ortiz and J. W. Kolar, "Design and Experimental Analysis of a Medium-Frequency Transformer for Solid-State Transformer Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 110-123, March 2017.

[4] L. Costa, G. Buticchi and M. Liserre, "Bidirectional series-resonant DC-DC converter with fault-tolerance capability for smart transformer," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.

[5] L. F. Costa, G. Buticchi and M. Liserre, "Modular Smart Transformer architectures: An overview and proposal of a interphase architecture," *2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Florianopolis, 2017, pp. 1-7.

[6] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa and Z. Zou, "The Smart Transformer: Impact on the Electric Grid and Technology Challenges," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46-58, June 2016.

[7] Y. Ko, A. Chub, L. Costa, M. Andresen and M. Liserre, "Smart transformer universal operation," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1609-1616.

[8] Z. Zou, G. Buticchi and M. Liserre, "Grid Identification and Adaptive Voltage Control in a Smart Transformer-fed Grid," in *IEEE Transactions on Power Electronics*, vol. pp, no. pp, pp. 1-1, 2018.

[9] T. Zhao, G. Wang, S. Bhattacharya and A. Q. Huang, "Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer," in *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1523-1532, April 2013.

[10] S. Pugliese, M. Andresen, R. A. Mastromauro, G. Buticchi, S. Stasi and M. Liserre, "A New Voltage Balancing Technique for a Three-Stage Modular Smart Transformer Interfacing a DC Multibus," in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2829-2840, March 2019.

[11] S. Pugliese, M. Andresen, R. Mastromauro, G. Buticchi, S. Stasi and M. Liserre, "Voltage balancing of modular smart transformers based on dual active bridges," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1270-1275.

[12] B. Zhao, Q. Song and W. Liu, "A Practical Solution of High-Frequency-Link Bidirectional Solid-State Transformer Based on Advanced Components in Hybrid Microgrid," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4587-4597, July 2015.

[13] K. Mainali, S. Madhusoodhanan, A. Tripathi, D. Patel and S. Bhattacharya, "Startup scheme for solid state transformers connected to medium voltage grids," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 1014-1021.

[14] X. Liu, L. Liu, H. Li, K. Corzine and T. Guo, "Study on the start-up schemes for the three-stage solid state transformer applications," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, 2012, pp. 3528-3532.

[15] X. Liu, H. Li and Z. Wang, "A Start-Up Scheme for a Three-Stage Solid-State Transformer With Minimized Transformer Current Response," in *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4832-4836, Dec. 2012.

[16] H. Dehghani Tafti *et al*., "Control of active front-end rectifier of the solid-state transformer with improved dynamic performance during precharging," *2017 Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, Singapore, 2017, pp. 1-6.

[17] M. Saeed, J. M. Cuartas, A. Rodríguez, M. Arias and F. Briz, "Energization and Start-Up of CHB-Based Modular Three-Stage Solid-State Transformers," in *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5483-5492, Sept.-Oct. 2018.

[18] L. B. Kehler, A. M. Kaminski, J. R. Pinheiro, C. Rech, T. B. Marchesan and R. R. Emmel, "Auxiliary power supply for solid state transformers," *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Monte Carlo, 2016, pp. 193-196.

[19] J. Liu, J. Yang, J. Zhang, Z. Nan and Q. Zheng, "Voltage Balance Control Based on Dual Active Bridge DC/DC Converters in a Power Electronic Traction Transformer," in *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1696-1714, Feb. 2018.

[20] F. An, W. Song, B. Yu and K. Yang, "Model Predictive Control With Power Self-Balancing of the Output Parallel DAB DC–DC Converters in Power Electronic Traction Transformer," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 1806-1818, Dec. 2018.

[21] J. Tian, C. Mao, D. Wang, S. Nie and Y. Yang, "A Short-Time Transition and Cost Saving Redundancy Scheme for Medium-Voltage Three-Phase Cascaded H-Bridge Electronic Power Transformer," in IEEE Transactions on Power Electronics, vol. 33, no. 11, pp. 9242-9252, Nov. 2018.

[22] T. Liu et al., "Start-Up Scheme for Dual-Active-Bridge Based 10KV Power Electronics Transformer in PV Application," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 7083-7087.

[23] J. Shi, W. Gou, H. Yuan, T. Zhao and A. Q. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," in *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1154-1166, April 2011.

[24] G. Wang *et al*., "Comparisons of different control strategies for 20kVA solid state transformer," *2011 IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, 2011, pp. 3173-3178.

[25] S. Pugliese, R. A. Mastromauro, F. A. Gervasio and S. Stasi, "Performance comparison of Simplified Feedback Linearization control with classical dual loop control for single-phase grid-connected inverters," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 6621-6626.

[26] S. Pugliese, R. A. Mastromauro, S. Stasi and M. Liserre, "CHB Converter DC Voltage Control Based on Feedback Linearization," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 4447-4452.

[27] F. Giuliani, N. Delmonte, P. Cova, A. Costabeber and A. Castellazzi, "Soft-starting procedure for dual active bridge converter," *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015, pp. 1-6.

Sante Pugliese (M'18) received the M.Sc. degree in automation engineering and the Ph.D. degree in electrical and information engineering from the Politecnico di Bari, Bari, Italy, in 2013 and 2018, respectively. In 2017, he was a Visiting Scholar with the Chair of Power Electronics, Kiel, Germany, where he is currently a Post-Doctoral Researcher. His research interests include power converters and control techniques for distributed power generation systems based on renewable energies.

Giampaolo Buticchi (S'10-M'13-SM'17) received the Master degree in Electronic Engineering in 2009 and the Ph.D degree in Information Technologies in 2013 from the University of Parma, Italy. In 2012 he was visiting researcher at The University of Nottingham, UK. Between 2014 and 2017, he was a post-doctoral researcher and Von Humboldt Post-doctoral Fellow at the University of Kiel, Germany. He is now Associate Professor in Electrical Engineering at The University of Nottingham

Ningbo China and the Head of Power Electronics of the Nottingham Electrification Center. His research focuses on power electronics for renewable energy systems, smart transformer fed micro-grids and dc grids for the More Electric Aircraft. He is author/co-author of more than 200 scientific papers and an Associate Editor of the IEEE Transactions on Industrial Electronics and of the IEEE Transactions on Transportation Electrification.
He is the Chair of the IEEE Industrial Electronics Society Technical Committee on Renewable Energy Systems.

Rosa A. Mastromauro (S'05 - M'10 - SM'18) received the M.Sc. and Ph.D degrees in electrical engineering from the Politecnico di Bari, Bari, Italy, in 2005 and 2009, respectively. Since 2005, she has been with the Power Converters, Electrical Machines, and Drives Research Team, Politecnico di Bari, where she was an Assistant Professor. Currently she is an Associate Professor at the University of Florence, Florence, Italy, and she is engaged in teaching courses in power electronics and electrical machines. Her research interests include power converters and control techniques for distributed power generation systems, renewable energies and transportation applications. Prof. Mastromauro is a member of the IEEE Power Electronics society, IEEE Industrial Electronics Society, IEEE Industrial Application Society, IEEE Power and Energy Society, IEEE Women in Engineering Society. She is Associate Editor of the IEEE Transactions on Industrial Electronics. She is a reviewer for IEEE conference proceedings and journals.

Markus Andresen (S'15-M'17) received the M.Sc. degree in electrical engineering and business administration in 2012 and the Ph.D degree in 2017 from the chair of power electronics at Christian-Albrechts-University of Kiel, Germany. In 2010, he was an intern in the Delta Shanghai Design Center at Delta Electronics (Shanghai) Co., Ltd., China and in 2017 he was a visiting scholar at the University of Wisconsin-Madison, USA. His current research interests include control of power converters and reliability in power electronics. Dr. Andresen was receipt of one IEEE price paper award on active thermal control of power electronics.

Marco Liserre (S'00-M'02-SM'07-F´13) received the MSc and PhD degree in Electrical Engineering from the Bari Polytechnic, respectively in 1998 and 2002. He has been Associate Professor at Bari Polytechnic and Professor at Aalborg University (Denmark). He is currently Full Professor and he holds the Chair of Power Electronics at Christian-Albrechts-University of Kiel (Germany). He has published over 300 technical papers (more than 100 of them in international peer-reviewed journals) and a book. These works have received more than 25000 citations. Marco Liserre is listed in ISI Thomson report "The world's most influential scientific minds".
He is member of IAS, PELS, PES and IES. He has been serving all these societies in different capacities and he has received 5 IEEE awards and 2 paper awards.

Silvio Stasi was born in Bari, Italy, in 1958. He received the M.Sc. degree from the University of Bari, Bari, Italy, in 1989 and the Ph.D. degree from Politecnico di Bari, Bari, Italy, in 1993 both in electrical engineering.
From 1990 to 1993, he was with the Electric Drives and Machines Group, Politecnico di Bari, where he carried out research on control and state and parameter estimation of electrical drives, and since November 2002, has been an Associate Professor of electrical machines and drives with the Department of Electrical and Information Engineering. His research interests include control of electric drives, fuzzy logic, neural networks, power electronics, and motor parameter estimation.